FUNDAMENTALS OF

BioMEMS and Medical Microdevices

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Chapter 2

Silicon Microfabrication

2.1 Hard Fabrication Considerations

Microfabrication is the process for the production of devices in the submicron to millimeter range. Often the fabrication techniques are divided into "hard" and "soft" manufacturing methods to describe the differences in materials and procedures. Many of the hard fabrication techniques for silicon and other ceramics are similar to those used for integrated circuit fabrication and will be reviewed in this chapter.

Prior to fabrication, the device needs to be designed and modeled. The design process may be a team approach, using the skills of mechanical, electrical, chemical, and biological engineers, and assisted with computer-aided design (CAD) and mathematical modeling tools. The goal is to outline a set of *process steps* that will result in the final device. The designer must also be aware of the abilities and limitations of the fabrication facility.

There are differences in research, prototype, and commercial application techniques based on equipment availablity, cleanliness of the fabrication facility, ability for mass production, and quality control.

For illustration purposes we will follow a silicon wafer through various process steps from resist application to etching, and finally to inspection with profilometry.* Along the way other processes and technical considerations will be introduced. More specialized techniques are accompanied by a review of their applications as gleaned from the current bioMEMS literature. Recommended textbook resources are listed at the end of the chapter, after the References section.

Soft fabrication techniques include molding, embossing, stamping, casting, and array patterning using polymers and biological substances, and other soft techniques include polymerization of 3D parts using light, surface modifications, and hydrogels. These are discussed in the next chapter because soft fabrication steps typically require different equipment and techniques than those of hard fabrication. In a university setting such equipment may be distributed among various research labs.

2.1.1 Traditional MEMS materials

The majority of MEMS devices are made from the same materials used for microelectronics, including, for example, single crystal silicon wafers, deposited layers of polycrystalline silicon (polysilicon) for resistive elements, aluminum, copper, and gold for conductors, silicon oxide for insulation and as a sacrificial layer (to allow *release* of moving parts), and silicon nitride and titanium nitride for

*University of Minnesota Nanofabrication Center.

electrical insulation and passivation. The silicon materials have high strength at small scales, which allows higher strain levels and less susceptibility to damage and fracture [Spearing, 2000].

For bioMEMS, traditional materials have been complemented with a host of polymers, including structurally rigid materials, hydrogels that may shrink and swell when exposed to environmental changes, and electroactive polymers (EAPs) that can change shape and structure when exposed to electrical stimuli.

Modification of polymeric backbone moieties, covalent modification of polymer surfaces for interaction with biological substances, and creation of hydrophobic or hydrophilic regions along a channel can be accomplished by chemical and radiative exposure. Surface modification may be helpful for transport, implementing electrokinetic effects, and immobilization.

Biological materials, including antibodies, DNA fragments, biotin-labeled serum albumin, and streptavidin-coated polystyrene beads can also be incorporated into devices. Nonetheless, silicon, dielectrics, metals, glass, and ceramics remain integral to if not the foundation for bioMEMS devices and are reviewed first.

2.1.2 Silicon

2.1.2.1 Microelectronics

Fundamental to the microelectronics revolution, silicon devices have largely replaced vacuum tubes except in certain high-power or high-frequency applications. Figure 2.1 shows the evolution of vacuum tubes (left) and semiconductor devices (right). Figure 2.2 shows a typical triode vacuum tube, the first point-contact transistor, junction transistor, integrated circuit, and the Intel Pentium microprocessor.

Early three-element vacuum tubes used a hot filament to emit electrons, and amplification was achieved by controlling grid and plate currents. Appearing in 1915, these served not only for early radio and television applications, but also for simple logic gates used in the first computers. They are still sought after by antique radio enthusiasts around the world!

The point-contact transistor was built in 1947 at Bell Laboratories (by Walter Brattain and John Bardeen, inclusive of the theoretical works of William Shockley), and consisted of bulk *n*-type germanium, *p*-type materials (doped semiconductor materials) and gold contacts. Shockley invented the bipolar transistor in 1948, and in 1959 the integrated circuit was invented.

Today's microprocessors have millions of transistors on a single chip. Bardeen, Brattain, and Shockley were awarded the Nobel Prize in Physics in 1956 for inventing the transistor and for semiconductor research [Casey, 1999].

2.1.2.2 Silicon, ICs, and MEMS devices

Microelectromechanical systems (MEMS) devices, largely made of silicon, use the fabrication techniques used in integrated circuit manufacturing. Figure 2.3

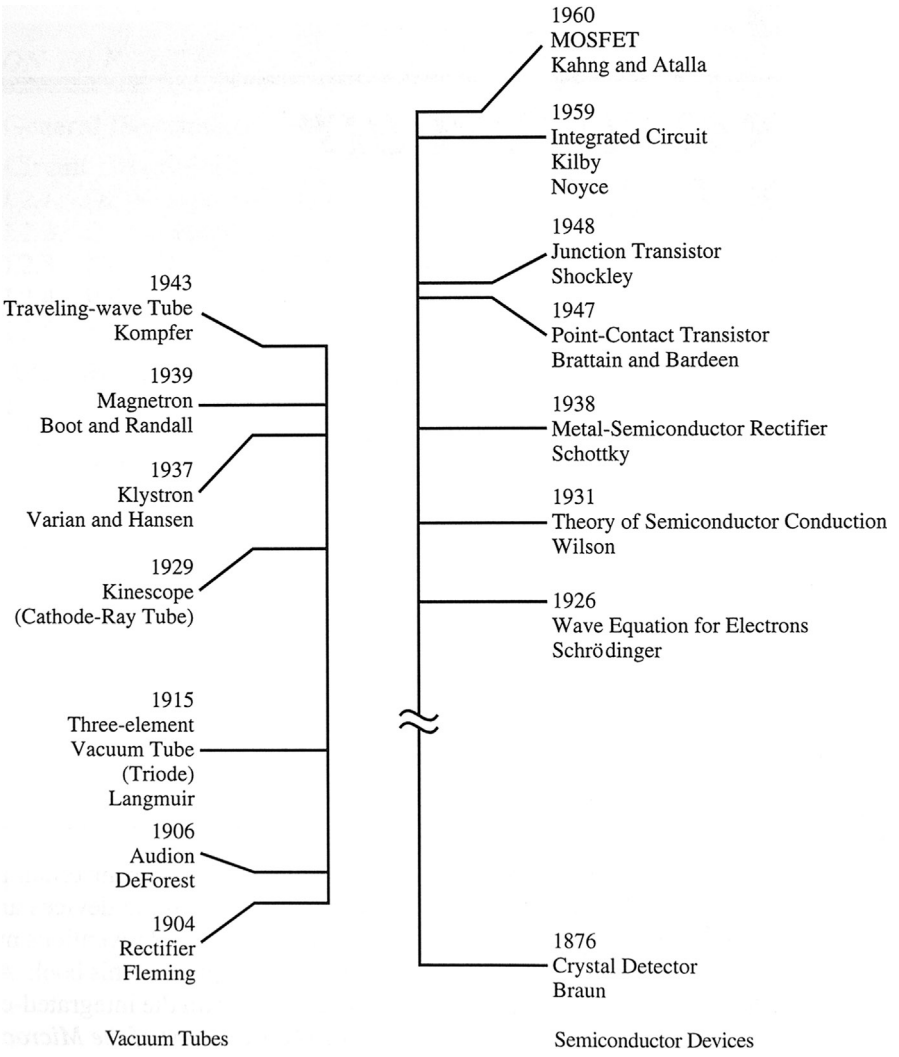

Figure 2.1 Family tree for vacuum tube devices (left) and semiconductor devices (right). [Reprinted with permission from Casey (1999), copyright John Wiley & Sons.]

shows the process steps for the manufacturing of silicon metal oxide semiconductor (MOS) integrated circuits.

Silicon wafers of varied diameters and crystal orientation are cut from long silicon boules and serve as device substrates. These are subjected to the application of a variety of thin films by thermal, chemical, and vapor deposition, epitaxial, or sputtering techniques. These include thermal silicon oxide, dielectric materials such as silicon dioxide and silicon nitride, polycrystalline silicon, and conductive metal films. Photolithography for pattern transfer, using masks and resists, interweave other process steps of deposition and etching (micromachining)

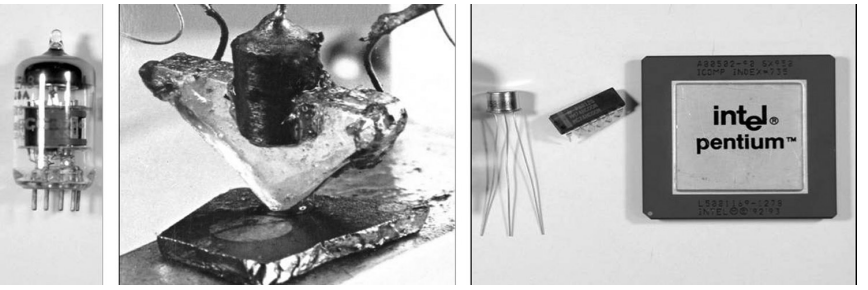

Figure 2.2 From left to right, a vacuum tube, the first point-contact transistor (courtesy of Lucent Technologies), a junction transistor, an integrated circuit, and the Intel Pentium microprocessor.

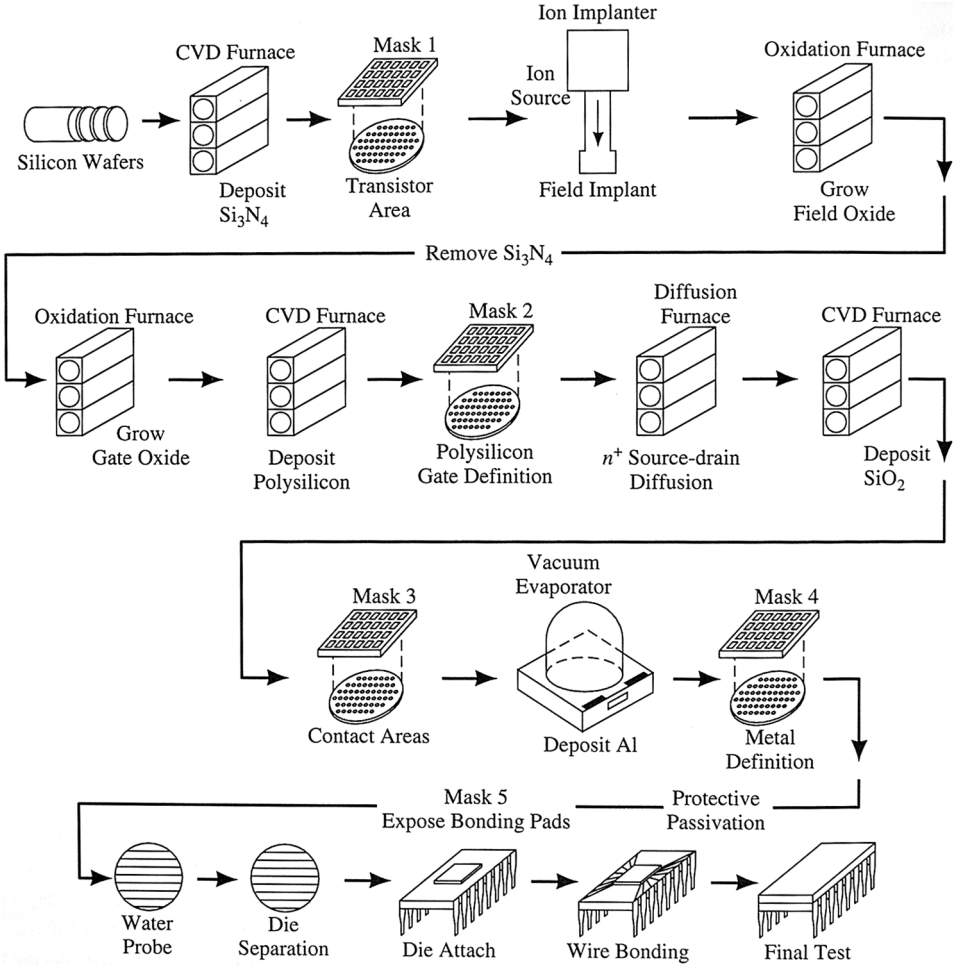

Figure 2.3 Manufacturing silicon MOS integrated circuits. [Reprinted with permission from Casey (1999), copyright John Wiley & Sons.]

to achieve 3D structures. Many bioMEMS devices incorporate silicon and use these same techniques.

2.1.2.3 Silicon crystals

While a complete discussion of the structure of materials, including intermolecular forces, atomic packing, and bonding is beyond the scope of this book, it is relevant to our discussion of fabrication techniques to review the basic concepts of crystal structures. Mitchell (2004) provides an excellent review of the properties and mechanics of materials, including metals and alloys, ceramics and glasses, composites and polymers.

There are fourteen types of crystal structures in nature (called *space lattices* or *Bravais lattices*) classified into seven *crystal systems* including cubic, orthorhombic, rhombohedral, tetrahedral, monoclinic, triclinic, and hexagonal. The cubic system (Fig. 2.4) for example, is composed of three space lattices or *unit cells*, including the *simple cubic* (SC), *body-centered cubic* (BCC), and *face-centered cubic* (FCC). Aluminum, copper, gold, and platinum all exhibit the FCC lattice.

The cubic structure is not close-packed, and has a large central space, or *interstitial space*. The interstitial space is vacant between atoms that may be occupied by a small impurity atom or alloying element.

Silicon is an element that exists in three forms: *crystalline*, *polycrystalline* (polysilicon), and *amorphous* (glassy). Single crystal silicon wafers may be used as a substrate material for MEMS and bioMEMS devices. Polycrystalline and amorphous silicon are reviewed below for use as thin films (which have thicknesses below 5 μm). Crystalline silicon forms a covalently bonded structure and coordinates itself tetrahedrally. Silicon (and germanium) crystallizes as two interpenetrating FCC lattices.

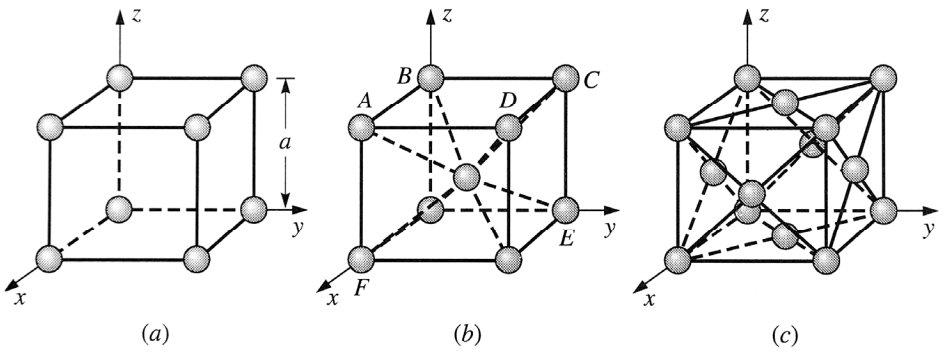

Figure 2.4 The cubic system is composed of three space lattices or *unit cells*, including (a) the simple cubic, (b) body-centered cubic, and (c) the face-centered cubic. [Reprinted with permission from Sze (1994), copyright John Wiley & Sons.]

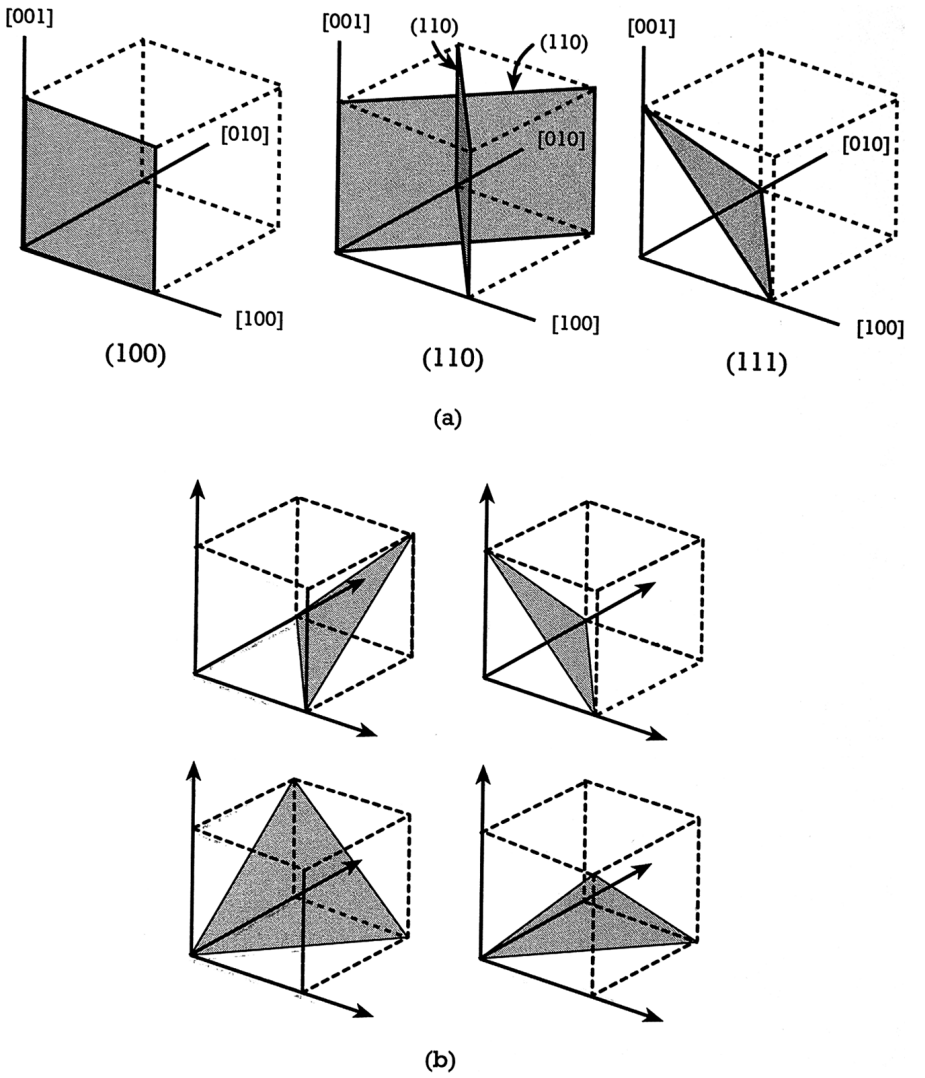

Figure 2.5 Miller indices for a simple cubic crystal. In (a) the three crystallographic planes and their Miller indices, as well as two equivalent (110) planes in the {110} set of planes are depicted. In (b) four of the eight equivalent (111) planes in the {111} family are shown. [Reprinted with permission from Maluf (2000), copyright Artech House.]

Crystal planes are important for electrical and etching properties, and are defined by the *Miller indices.* A simple cubic crystal and its Miller indices are shown in Fig. 2.5.

The silicates are made up of base units of silicon and oxygen and may be either crystalline or amorphous. They are complex structures that can contain additional atoms such as Mg, Na, and K.

2.1.2.4 Single crystal silicon

The silicon boule is an elongated growth of a single silicon crystal manufactured by techniques such as the Czochralski process, chemical-vapor deposition, or the float-zone process. A seed crystal determines the final crystal orientation as defined by the various planes that can be drawn through adjacent or opposing silicon atoms in the cubic structure. The Miller indices, in their most simple context, serve to identify and label these orientations in the silicon wafers cut from the original boule.

In the Czochralski technique a silicon crystal is gradually pulled upward by a rod connected to a rotating seed crystal that rests initially upon the surface of stirred molten silicon in a graphite crucible. The entire unit is housed in a silica enclosure with a controlled inert atmosphere. The rotating seed-bearing rod is pulled back a few millimeters a minute, allowing the crystal boule to grow. The boule is then cut into wafers of defined diameters and thicknesses.

2.1.2.5 Electronic-grade silicon

Silicon is the most used semiconductor element in electronics and bioMEMS. Electronic-grade silicon (EGS) is fabricated by the following steps:

(1) Quartzite is placed in a furnace with carbon-releasing materials, and reacts as shown, forming metallurgic-grade silicon (MGS):

$$SiO_2(s) + 2C(s) \xrightarrow{\text{heat}} Si(s) + 2CO(g). \tag{2.1}$$

(2) MGS is then treated with hydrogen chloride to form trichlorosilane:

$$Si + 3HCl \xrightarrow{\text{heat}} SiHCl_3(g) + H_2(g). \tag{2.2}$$

(3) Fractional distillation reduction with hydrogen produces EGS:

$$SiHCl_3(g) + H_2(g) \xrightarrow{\text{heat}} Si(s) + 3HCl(g). \tag{2.3}$$

2.2 Lithography

The basic concept of photolithographic surface micromachining is shown in Fig. 2.6, where a patterned lithographic mask is made and used to expose a photoresist and silicon dioxide (sacrificial layer) coated substrate such as silicon or glass. Light polymerizes the photoresist protecting those exposed areas from being etched away, and a structural material like polycrystalline silicon is deposited. More lithography patterns the structural material, which is then etched. Finally the sacrificial layer is etched away, leaving the surface detail. Each of these steps is discussed below.

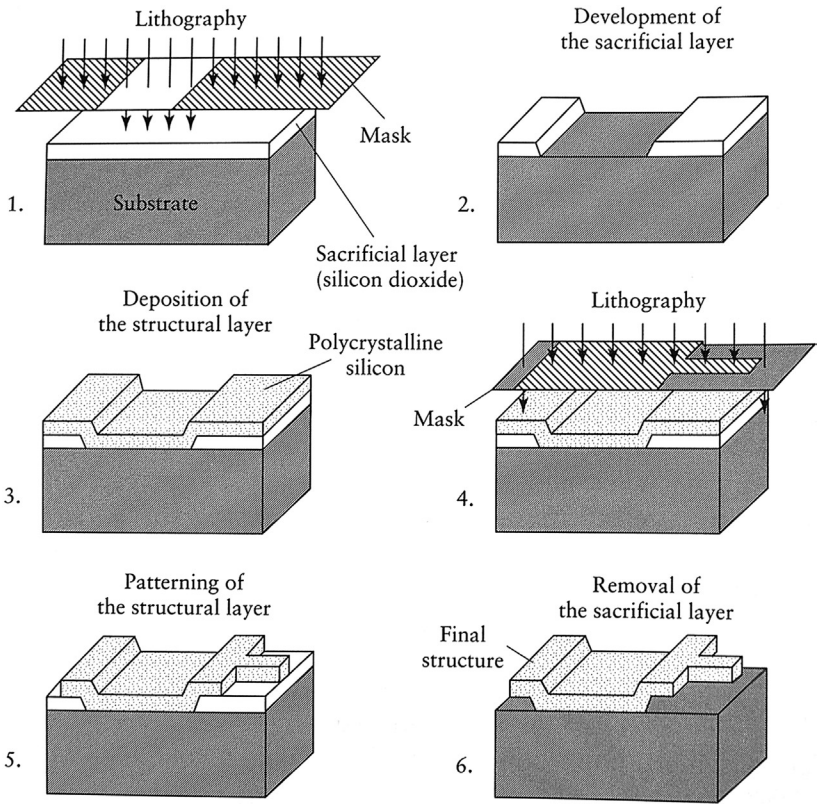

Figure 2.6 Processing steps for surface micromachining. (a) A patterned lithographic mask is made and used to expose a photoresist and silicon dioxide (sacrificial layer) coated substrate such as silicon or glass; (b) light polymerizes the photoresist protecting those exposed areas from being etched away; (c) a structural material like polycrystalline silicon is deposited; (d) more lithography patterns the structural material; (e) the structural material is then etched; and finally (f) the sacrificial layer is etched away, leaving the surface detail. [Reprinted with permission from Fatikow and Rembold (1997), copyright Springer.]

2.2.1 Mask creation

A mask is created first (Fig. 2.7), and this serves as a "stencil" to generate a pattern on a resist-coated surface. Both glass and quartz plates can be used since they are transparent to ultraviolet light (UV) and may be placed in direct contact or proximity contact (10–20 μm) above the surface. Masks may be produced by means of a CAD-driven *x-y* stage photo exposure process.

Projection printing uses a lens focusing system that allows 1:5 or 1:10 reduction, which makes fabrication of the mask easier and increases the life of the mask.

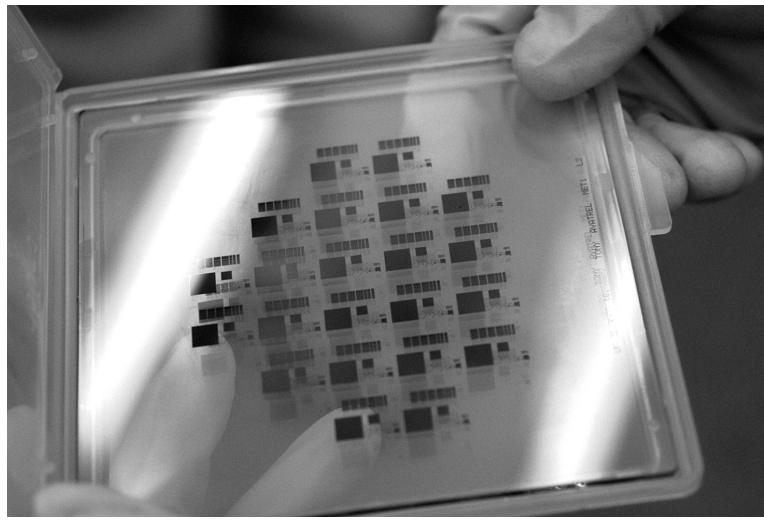

Figure 2.7 Lithographic mask.

2.2.2 Wafer cleaning

Wafers may come already cleaned, and are typically ordered based on dimensions and doping, and if so desired, with thin-film coatings already applied. A typical wrapped package of wafers is shown in Fig. 2.8, and a single wafer in Fig. 2.9.

Wafer cleaning occurs in the clean room, and may include RCA1 and RCA2[†] cleaning protocols. The RCA1 cleaning steps include mixing one part NH_3 with five parts deionized water, heating them to boiling, then adding one part H_2O_2, and immersing the wafer for ten minutes to remove dirt. The RCA2 cleaning steps include mixing one part HCL and six parts deionized water, heating to boiling, then adding one part H_2O_2, and immersing the wafer for ten minutes to remove metal ions. Both methods leave a thin oxide surface coating. Other methods include vapor cleaning, ultrasonic agitation, and polishing plasma.

2.2.3 Thermal silicon dioxide

Thermal oxidation is used for growing oxide layers below 1-μm thick [Fig. 2.10(a)]. Thermal oxidation of silicon can be accomplished in at least three ways, including dry oxidation, wet oxidation, and pyrogenic oxidation. Thermal oxidation may be performed by a *rapid-thermal-annealing* process whereby the wafer is heated rapidly, and may be useful in growing an oxide layer. The SiO_2 layer can be used

[†]Standard cleaning procedures.

Figure 2.8 Silicon wafers as delivered from the manufacturer.

as an insulating layer, a mask, diffusion barrier, and as sacrificial material. Oxidation in steam is faster, but produces a poorer material:

$$\mathrm{Si(solid)} + \mathrm{O_2(gas)} \xrightarrow{900-1200^{\circ}\mathrm{C}} \mathrm{SiO_2(solid)} \tag{2.4}$$

and

$$\mathrm{Si(solid)} + 2\mathrm{H_2O(gas)} \longrightarrow \mathrm{SiO_2(solid)} + 2\mathrm{H_2(gas)}. \tag{2.5}$$

Figure 2.9 Polished silicon wafer.

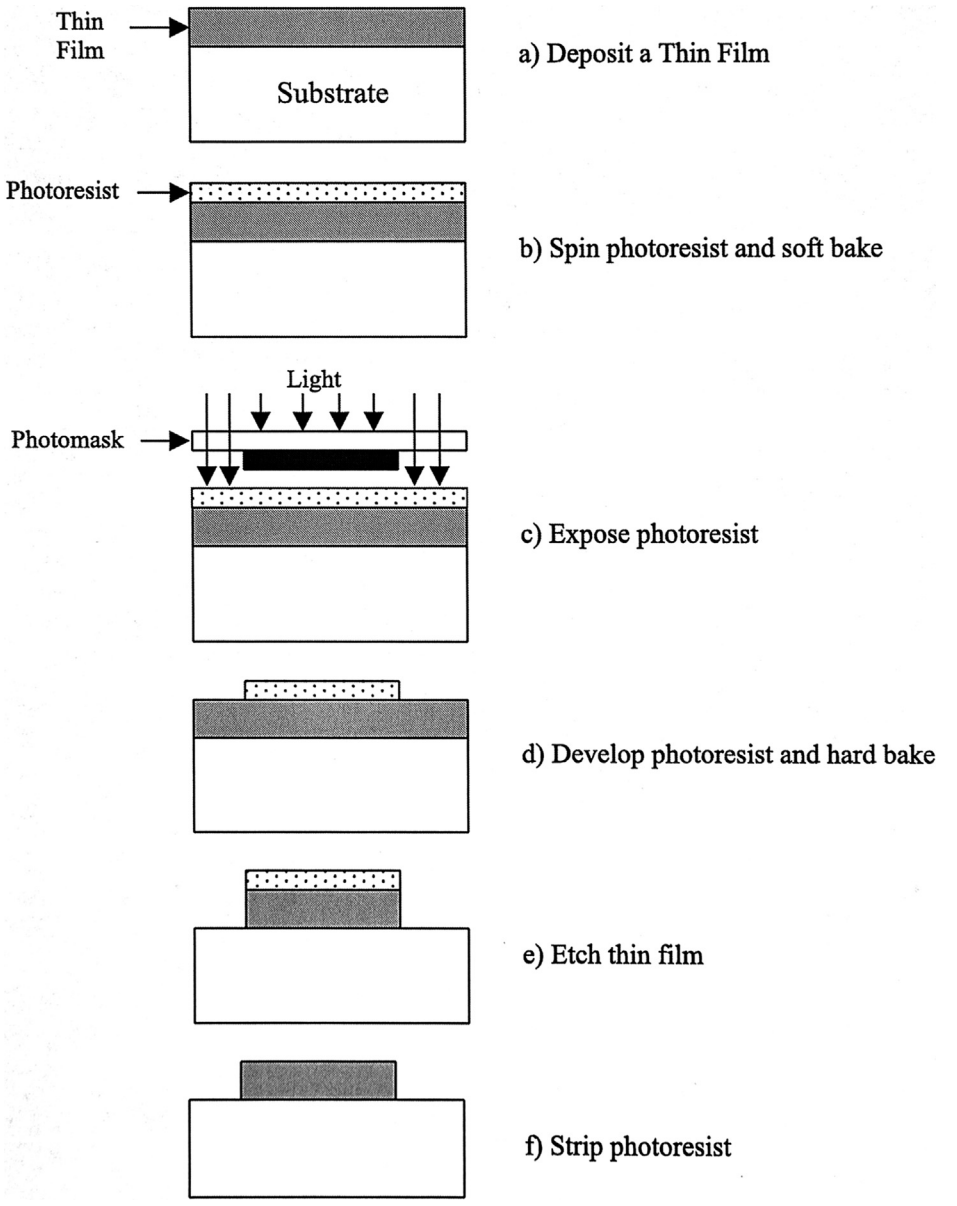

Figure 2.10 Photolithographic steps with a positive photoresist. [Reprinted with permission from Baldi and Ziaie (2004), copyright Elsevier.]

More commonly thermal oxidation is accomplished in an atmospheric furnace, allowing sustained high temperatures (Fig. 2.11). Silicon wafers are placed upright in an appropriate carriage and loaded into the furnace (Fig. 2.12).

Thermal oxidation of silicon generates compressive stress in the silicon dioxide film, and layers greater than 1 μm may cause bowing of the underlying substrate.

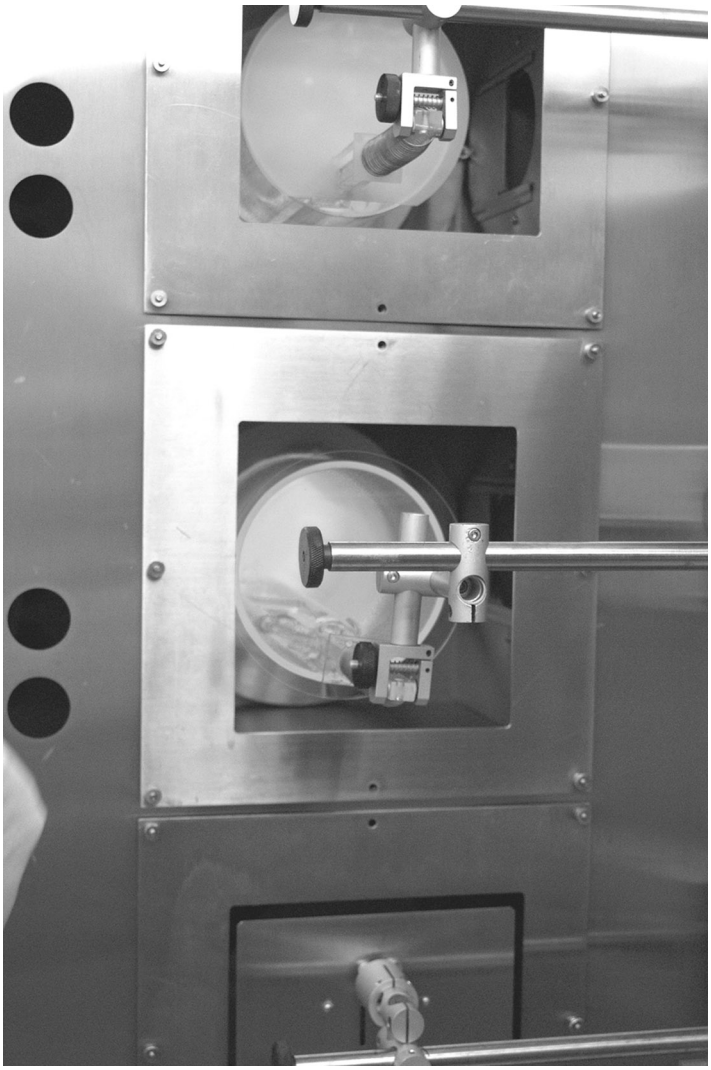

Figure 2.11 Atmospheric furnace.

2.2.4 Resist application

Once the thermo silicon oxide layer is created, the wafer is ready for resist application [Fig. 2.10(b)]. A resist is a solution of a photosensitive polymer, or *photoresist.* The photoresist is dispensed onto the wafer and spun at high speed (∼3000 RPM), creating a uniform layer (Fig. 2.13). This *spin-casting process* leads to smooth films (rms roughness of less than 1 nm). A good resist must have good adherence to the silicon, high sensitivity, and high contrast to UV exposure, good etching resistance to etch solutions, good resolution, easy processing, high purity, long shelf life, minimal solvent use, low cost, and high

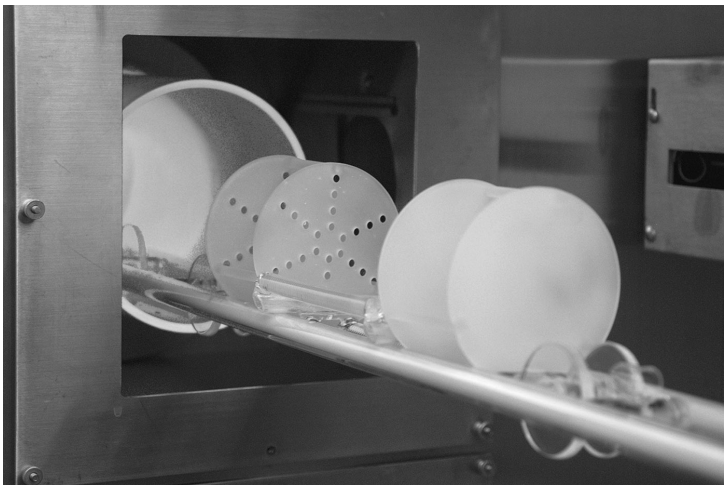

Figure 2.12 Atmospheric furnace loading rack.

thermal glass-transition temperature. The coating thickness depends on the fineness of the lines and spaces to be resolved, and feature sizes as small as 0.18 μm require thicknesses of 1 μm ± (10 Å). Reflection spectroscopy may be used to monitor the resist thickness. The wafer is then "soft baked" at 75–100°C for about ten minutes to remove solvents and improve adhesion (Fig. 2.14).

Both positive and negative resists can be chosen, depending on whether it is desirable to have the opaque regions of the mask protect the resist, and hence the substrate below, or having the transparent regions protect the resist when exposed to UV. Areas where the resist is removed are ultimately etched. Remember that "positive protects."

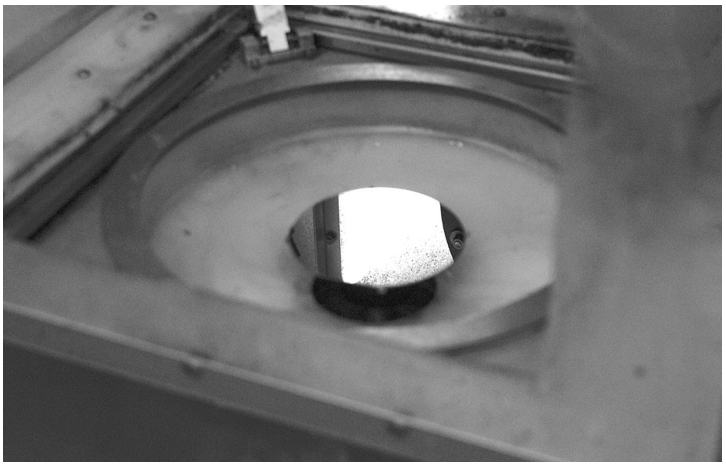

Figure 2.13 Spin application of resist coating.

Figure 2.14 Silicon wafer soft and hard baking plates.

Positive resists include poly(methyl methacrylate) (PMMA), and a two-part system, diazoquinone ester plus phenolic novolak resin (DQN). Negative resists include SU-8, bis(aryl)azide rubber, and Kodak KTFR [Madou (2002)].

2.2.5 UV exposure

The mask is placed into a cassette and then into the UV exposure machine (Fig. 2.15). The resist-coated wafer is placed on an adjustable tray, and micrometer controls and a view-screen allow for precise alignment (or registration) of the mask onto the

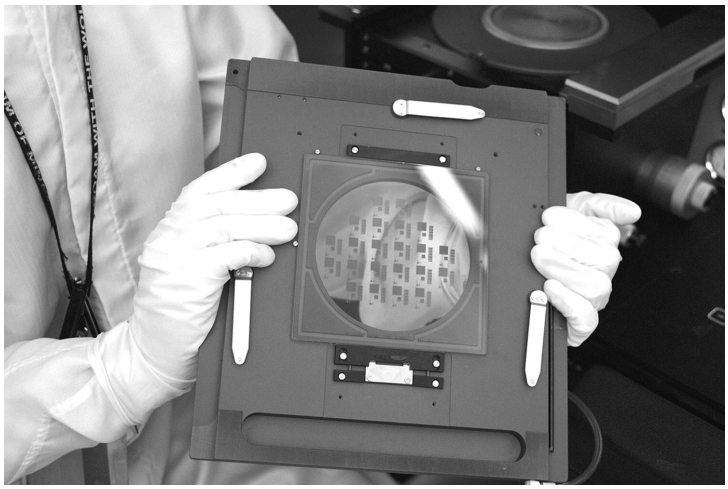

Figure 2.15 Mask and carriage.

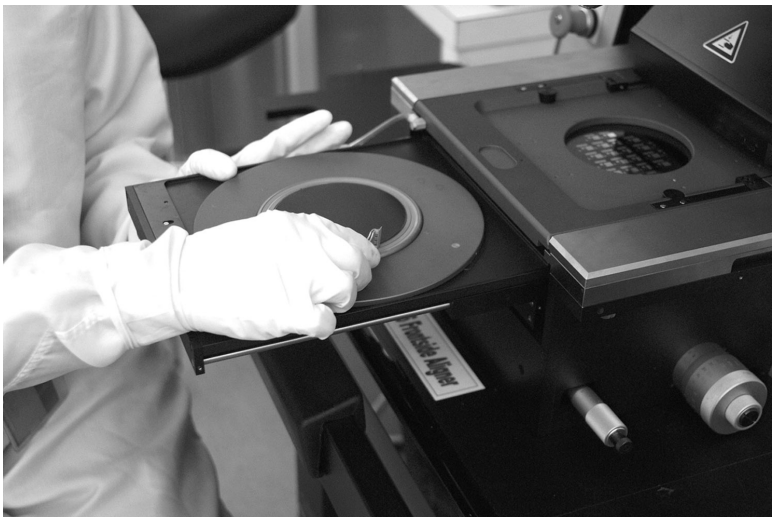

Figure 2.16 Mask and carriage positioned for UV exposure.

wafer based on fiducial marks on the mask (crosshairs or optical vernier), (Fig. 2.16). The alignment process is crucial for forming complex multilayer structures and for fabrication of miniaturized devices.

Near-UV light at 350–500 nm is used for exposing the wafer [Fig. 2.10(c)]. There are mercury lamps optimized for the g-line at 435 nm, and for the i-line at 365 nm. Menu-driven machine settings assist in the process (Fig. 2.17). The wafer is then exposed to UV light (at the g-line) as programmed (Fig. 2.18).

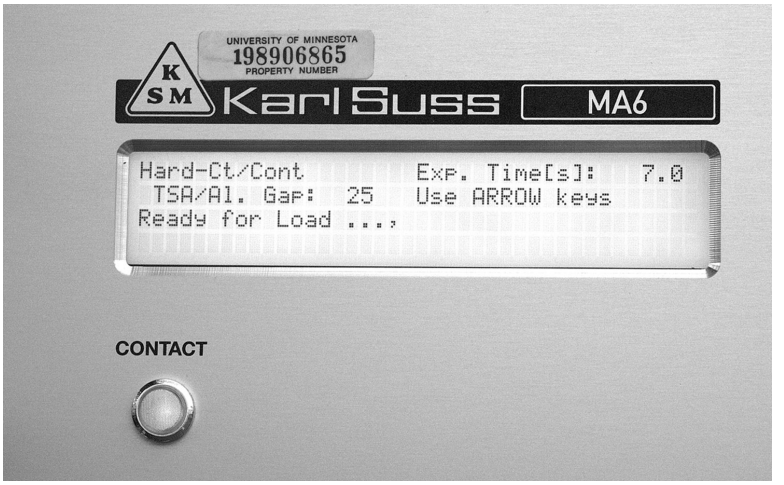

Figure 2.17 UV exposure control panel with exposure duration setting.

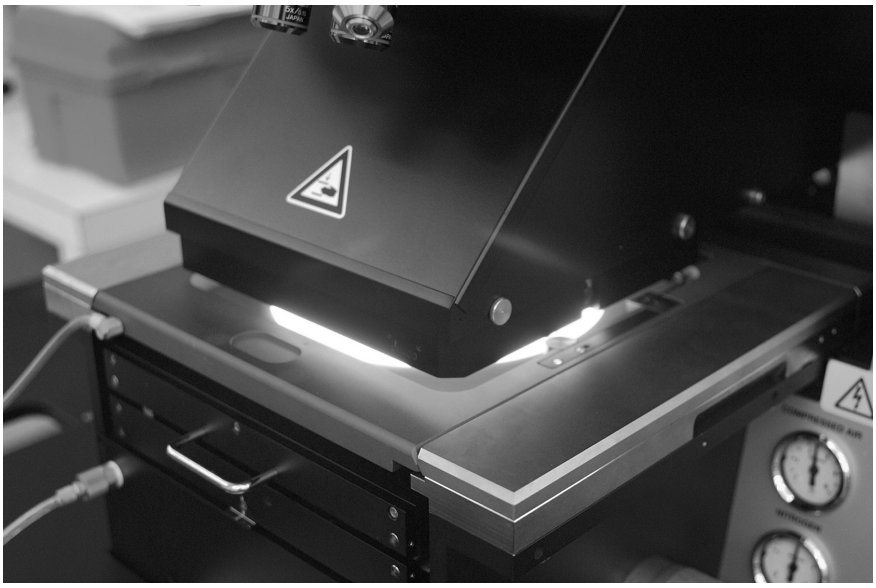

Figure 2.18 Timed UV exposure.

2.2.6 Development

After UV light exposure, the wafer is developed. With a positive resist, UV exposure causes the polymer to weaken and become more soluble in the developer. The converse is true for negative resists.

Positive resists typically develop in KOH, and other aqueous alkaline solutions, and negative resists in organic solutions. Post-baking or "hard baking" is done prior to etching or electroplating, and sometimes it is done mid-etching to prevent resist breakdown [Fig. 2.10(d)]. Controlled baking is necessary to prevent unwanted breakdown or excessive hardening of the resist. Figure 2.19 shows the development step. The silicon wafer with developed pattern is shown in Fig. 2.20.

Once the resist pattern is developed and the underlying oxide is etched away, options are available for *etching* and include dry and wet techniques, as well as additive processes such as chemical and physical vapor deposition, epitaxial growth, and sputtering [Fig. 2.10(e)]. The resists themselves are either stripped away at some point or may become part of the device. Some dry resist films (that come in rolls) and polyimides are left on and become part of the device. Polyimides, for example, can serve as low-dielectric insulation layers or flexible hinges.

Resist stripping can be accomplished by first removing most of the resist with an oxygen plasma ashing, then applying a 3:1 mixture of H_2SO_4 and H_2O_2 (acid Piranha solution) kept heated to about 120°C. The substrate is then rinsed and dried [Fig. 2.10(f)].

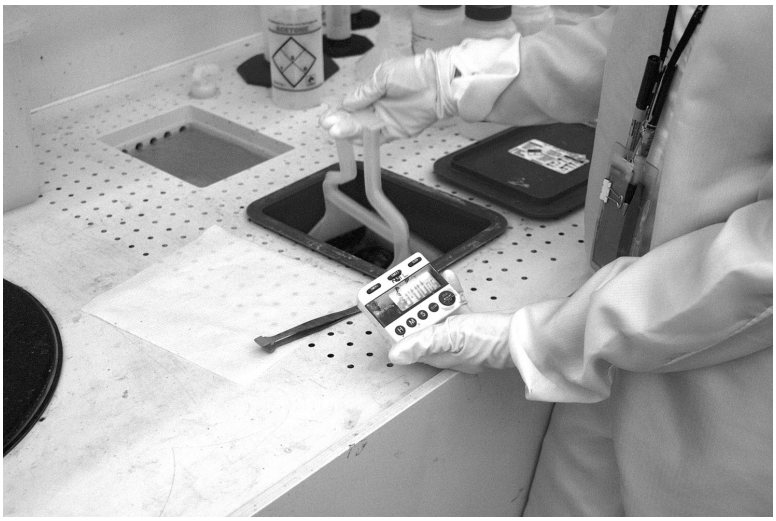

Figure 2.19 Manual developing of UV exposed wafer.

2.2.7 Technical considerations

2.2.7.1 Terminology

The lithography techniques discussed above are also used with materials other than silicon, and it is worth spending some time reviewing the terminology and physics of the process.

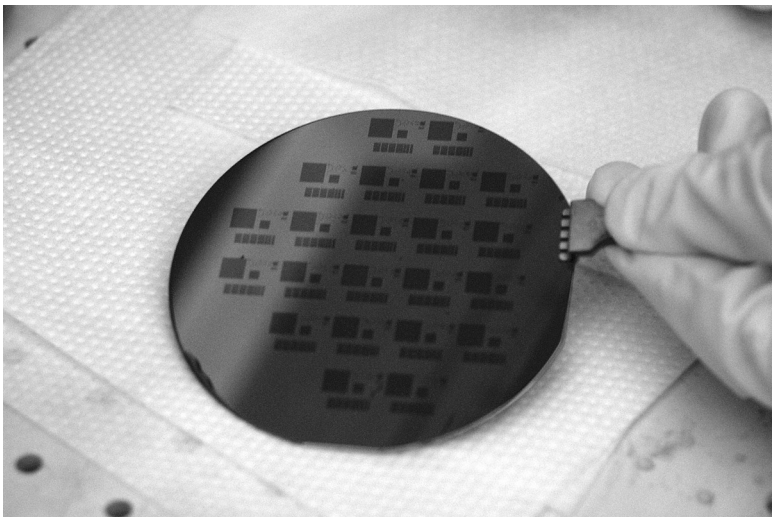

Figure 2.20 Resulting resist pattern after development.

C*ritical dimension* is the smallest feature size to be produced; *resolution* is the smallest line width to be consistently patterned; *line width control* refers to dimensions that must be controlled within $\pm 20\%$ of the minimum feature size; and *high intrinsic resist sensitivity* is the photochemical quantum efficiency:

$$\Phi = \frac{\text{Number of photo-induced events}}{\text{Number of photons absorbed}}, \tag{2.6}$$

where the numerator could be the number of molecules converted to photoproduct, and the denominator the number of photons required for completing the conversion. *G-value* is the number of polymer scissions or cross-links per 100 eV of absorbed energy. *Resist profile* is the duration of exposure, scattering, positive versus negative resist, and solvent choice, all of which affect the edge profile [Madou (2002)].

2.2.7.2 Theoretical limits to resolution

Line width measurements can be accomplished with scanning electron microscopes (SEM) and other devices. Contact and proximity resolution are limited by: (1) diffraction of light at the edge of an opaque feature, (2) alignment of wafer to mask, (3) nonuniformities in wafer flatness, and (4) contamination. The theoretical resolution (contact or proximity) is as follows:

$$R = b_{\min} = \frac{3}{2}\sqrt{\lambda\left(s + \frac{z}{2}\right)}, \tag{2.7}$$

where

$b_{\min}$ is half the grating period and the minimum feature size transferable,
s is the gap between the mask and the photoresist surface,
λ is the wavelength of the exposing radiation, and
z is the photoresist thickness.

If s is about 0, $\lambda = 400$ nm, and $z = 1$ μm, then R is approximately 1 μm. Shorter wavelengths, smaller gaps, and thinner resist layers improve resolution.

2.2.7.3 Future needs

Improving resolution is important as the emphasis on smaller bioMEMS devices increases. Moore's Law[†] states that the number of transistors per square centimeter roughly doubles every two years without an increase in cost. This will be limited at about the critical dimension of 30 nm when quantum effects take over. BioMEMS

[†]Gordon Moore was an inventor of the integrated circuit, and is Chairman Emeritus of Intel Corporation.

devices are not only limited by quantum effects, but also by difficulties in fabricating both electronic and nonelectronic components, including microfluidic components on the same substrate without one process step harming another. Traditionally, MEMS devices (with some exceptions) have been fabricated by having required electronics as separate chips. Application-specific integrated circuit (ASIC) chips can be program-designed and fabricated at low cost. These relatively compact chips may include microcontroller functions, logic, memory, analog-to-digital (AD) and digital-to-analog (DA) converters, and communication interfaces.

When considering implanted devices, miniaturization may be paramount for certain locations and to minimize biofouling. Integration by either coproduction on the same substrate or improved hybridization (so as to minimize interconnections) needs to be considered. This is especially for implanted devices requiring in-line detection schemes. Achieving higher resolution may require the use of x-ray and charged-beam lithography.

2.3 Etching Methods

2.3.1 Available techniques

After the silicon wafer has been patterned with a resist, it is necessary to remove (*subtractive* processes) or add material to it (*additive* processes). To remove material, both *dry etching* with *plasma methods* and *wet etching* with chemical liquids can be performed.

Dry etching includes *glow discharge* techniques using diode setups and *ion beam techniques* using triode setups. Glow discharge includes plasma etching (PE), reactive ion etching (RIE) and physical sputtering (PS). Ion beam includes ion beam milling (IBM), reactive ion beam etching (RIBE), and chemical-assisted ion beam etching (CAIBE). Deep reactive ion etching (DRIE) with the Bosch Process is a method for building high-aspect-ratio parts, and uses inductively coupled plasma.

Etching profiles are important and include isotropic (poor directionality) and anisotropic (good directionality) techniques, the latter producing more vertical walls. Each has its advantages and disadvantages. PE occurs at relatively lower energy and higher pressure (less vacuum), and is isotropic, selective, and less prone to cause damage. RIE is more middle ground in terms of energy and pressure, with better directionality. PS and IBM rely on physical momentum transfer from higher excitation energies and very low pressures, and result in poor selectivity with anisotropic etching and increased radiation damage.

2.3.2 Plasma etching (PE)

Simple PE uses a dc diode setup in which argon is held at low pressure between a negative cathode and positive anode (Fig. 2.21). Cathode and anode "glow bands," as well as "negative glow" bands, the latter producing the principle plasma used

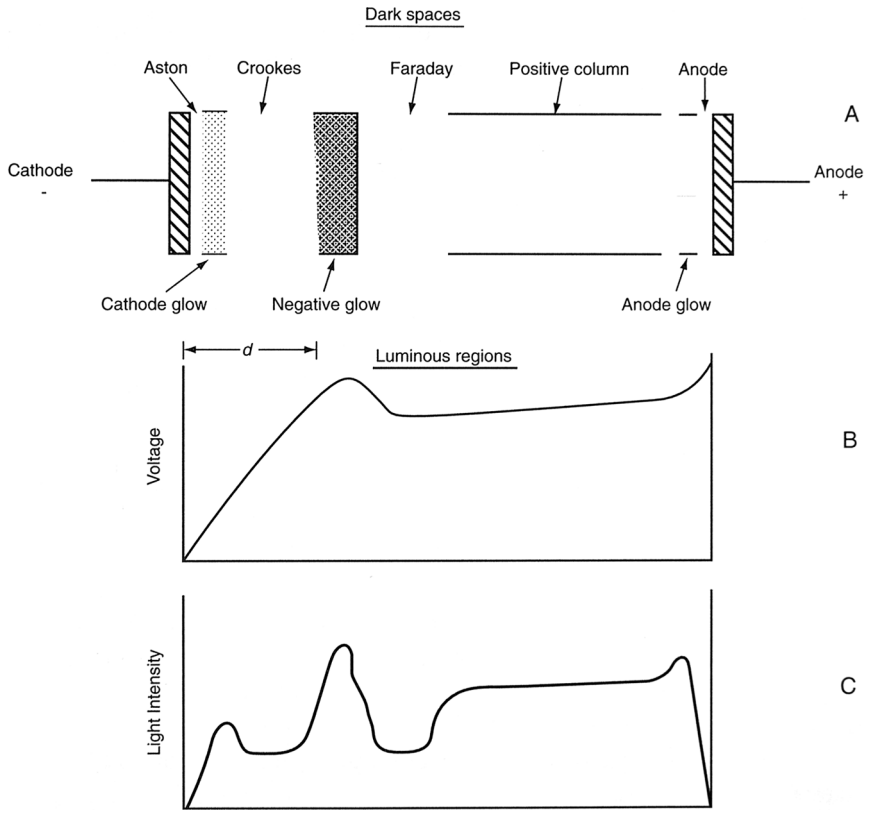

Figure 2.21 (a) Glow discharge in a dc diode system; (b) the potential distribution; and (c) light intensity distribution. [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group.]

for etching silicon. When this plasma bombards a surface, the impinging ions erode or sputter-etch the surface by momentum transfer. There is benefit derived from the etching, as well as from making use of the sputtered material. The reaction mechanism for the plasma etching process is shown in Fig. 2.22.

2.3.3 Reactive ion etching (RIE)

RIE can be accomplished with radio frequency (RF) generated plasma. An RF voltage is applied between the electrodes, causing free electrons to oscillate and collide with gas molecules, thus plasma is produced (Fig. 2.23). Lower pressures (10 versus 40 mTorr) are required compared to dc plasma, and both dielectrics and metals can be etched. RF plasma consists of positive cations, negative anions, radicals, and photons. When the wafer is placed on the cathode, reactive ion etching sputter occurs. Performance is enhanced with high quantities of low-energy ions and radicals at low pressures.

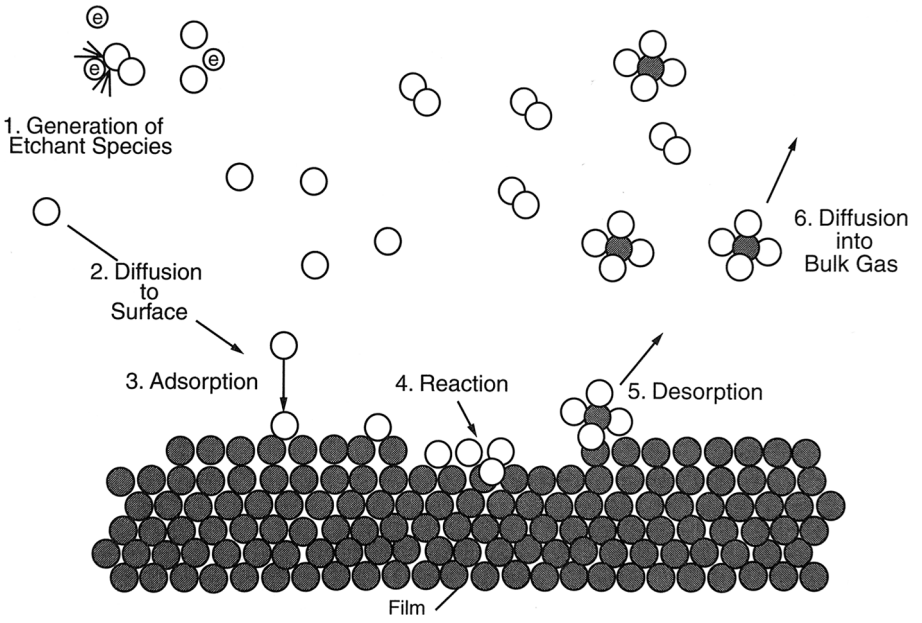

Figure 2.22 Primary process occurring in a plasma etch process. [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group.]

Figure 2.24 shows placement of our silicon wafer into the RIE machine. The lid is vacuum-sealed and the glow discharge (a remarkable blue color) is observed through the transparent port. MEMS devices might take up to an hour to complete; ICs may take only minutes. Gases present include SF_6 (sulfur hexaflouride) plus oxygen, which prevents etching from slowing down by keeping nonresist areas

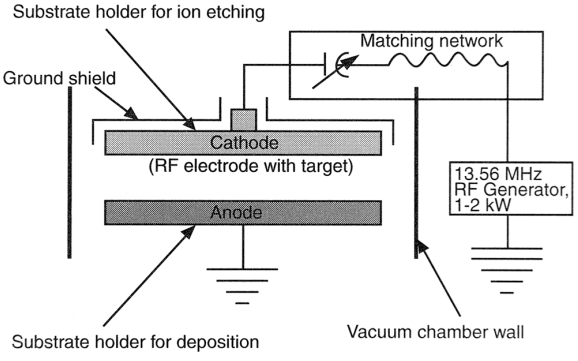

Figure 2.23 Two-electrode diode setup for RF ion sputtering (substrate on cathode target) or sputtering deposition (substrate on anode for deposition). [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group.]

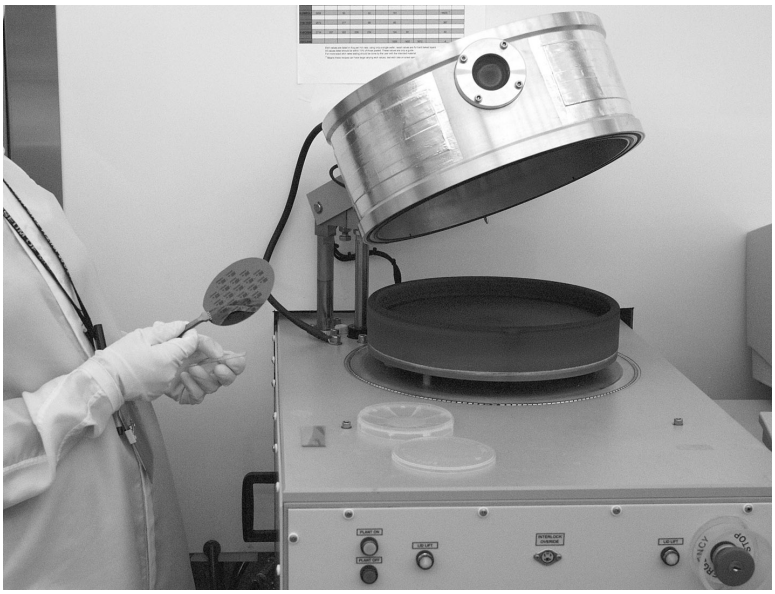

Figure 2.24 Placement of the silicon wafer into the RF RIE machine.

free of etch by-products). The vacuum exits to a scrubbing system for environmental safety. The etched wafer is shown in Fig. 2.25. The resist is then stripped (Fig. 2.26), and the wafer inspected in a profilometer (Fig. 2.27), and the output recorded (Fig. 2.28).

Other RIE machines are available, including one with chlorine gas as the reactive gas for aluminum etching. If a device requires electrical contacts for example,

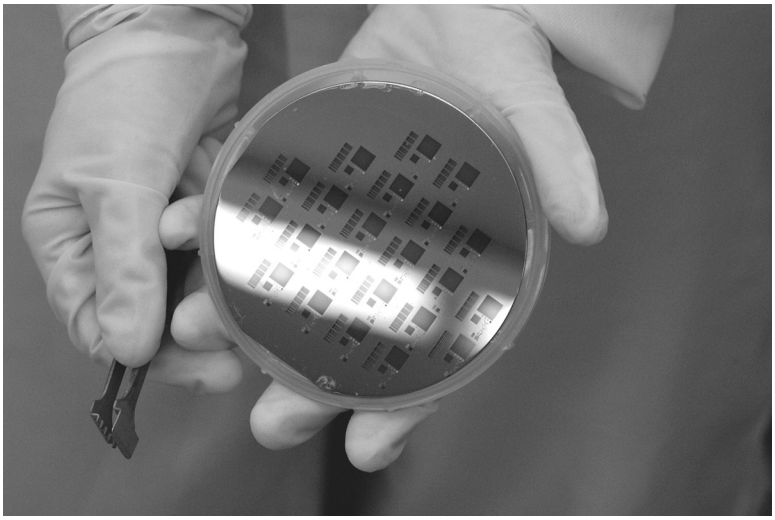

Figure 2.25 Silicon wafer after etching in RIE.

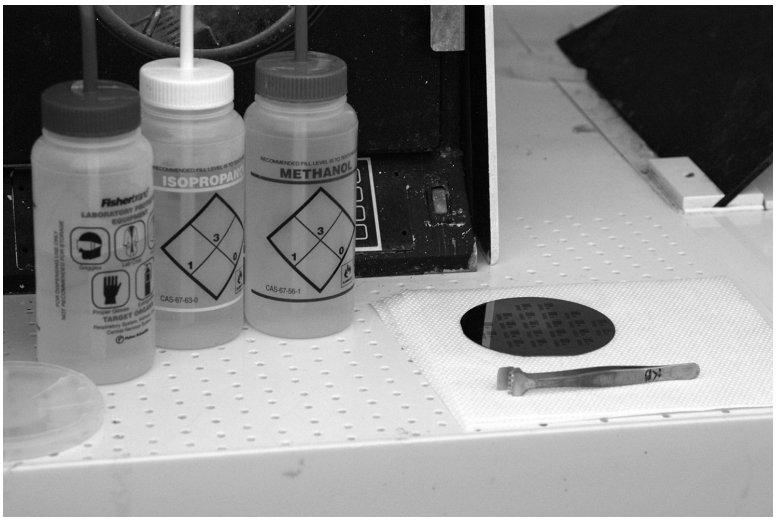

Figure 2.26 Solutions for stripping resist.

a wafer could be coated with aluminum, patterned, and then etched in this machine, leaving lines and contacts for bonding leads.

2.3.4 Physical sputtering (PS)

Bombarding a surface with inert ions (e.g., argon) has an effect related to the kinetic energy of the incoming particles. At energies <3 eV particles are simply

Figure 2.27 Profilometer for measuring surface features, including depth and width of etched structures.

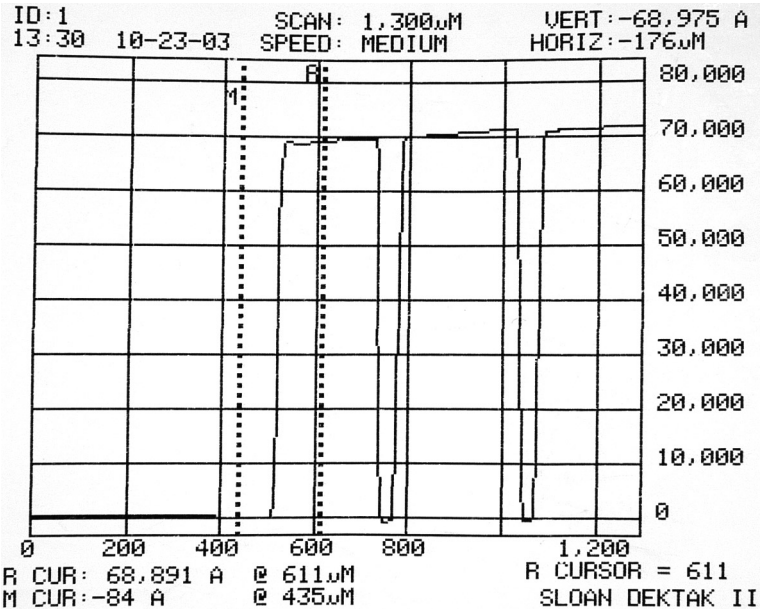

Figure 2.28 Typical profilometer output graph.

reflected or absorbed. At surface energies between 4–10 eV, some surface sputtering occurs. At surface energies of 10–5000 eV momentum transfer causes bond breakage and ballistic material ejection across the reactor to the collecting surface. A low pressure and long mean-free path are necessary to prevent the material from redepositing. Implantation (doping) occurs at 10,000–20,000 eV.

2.3.5 Ion beam milling (IBM)

A magnetically enhanced IBM triode setup is shown diagrammatically in Fig. 2.29. A hot filament serves as an electron source in an inert gas environment such as argon. Ions are extracted from the upper chamber by the grid, formed into a beam, accelerated, and fired into the lower chamber, where they hit the target. An example of an IBM is shown in Fig. 2.30.

2.3.6 Reactive ion-beam etching (RIBE) and chemical assisted ion-beam etching (CAIBE)

Both RIBE and CAIBE occur in triode setups, but unlike IBM, ion-surface interactions promote etching. In RIBE, reactive ions etch the surface directly, whereas in CAIBE, ion bombardment induces a reaction by making the surface more reactive for neutral plasma species. In effect, ions clear the surface of film-forming

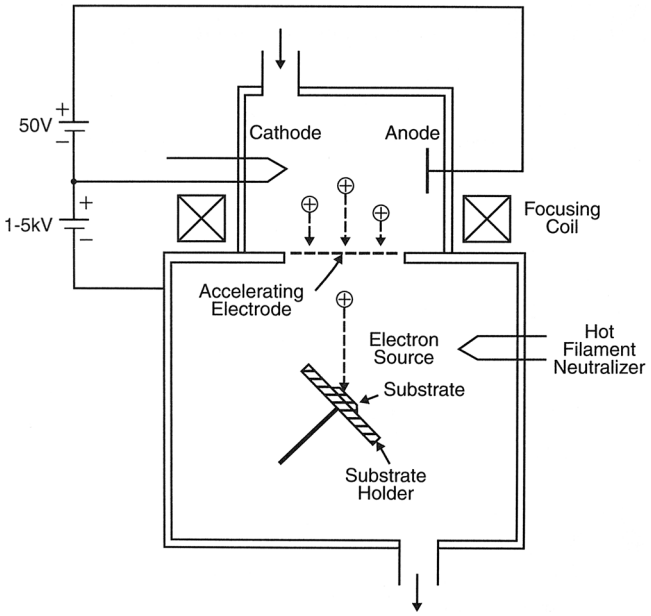

Figure 2.29 Ion-beam milling triode apparatus. [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group.]

Figure 2.30 Ion mill.

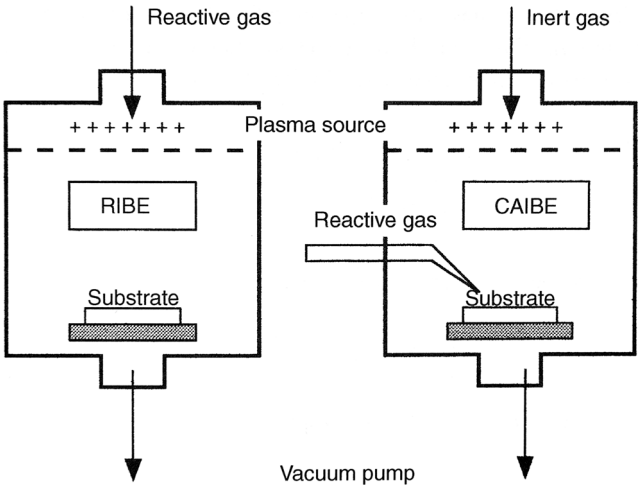

Figure 2.31 Chemically assisted ion-beam etching (CAIBE) compared with reactive ion-beam etching (RIBE). [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group.]

reaction products that allows etching with reactive neutrals to proceed in the cleared areas. In RIBE, the reactive ions come from the ion source itself, whereas in CAIBE, a reactive gas such as Cl_2 is flowed over the substrate (Fig. 2.31). CAIBE achieves highly anisotropic etch profiles with smooth vertical sidewalls.

2.4 Thin-Film Deposition Processes

Thin-film application is an additive process. Some important thin films include thermal silicon oxide, silicon dioxide (SiO_2), polysilicon, silicon nitride (Si_3N_4), phosphosilicate glass (PSG), and metal films. Thermal silicon dioxide coatings were described in Sec. 2.2.3. Physical-vapor deposition and chemical-vapor deposition are described here. Another technique is epitaxial growth, or growth of a single crystal layer on a substrate (serving as a "seed") one layer of atoms at a time. Vapor-phase epitaxy and molecular-beam epitaxy may be employed for this purpose.

2.4.1 Physical vapor deposition (PVD)

Physical vapor deposition is the production of a condensible vapor by physical means and its deposition on a substrate as a thin film. Like chemical-vapor deposition (CVD) discussed below, the deposition species are atoms or molecules or a combination of these. Material is transported in vapor form from a source to a substrate through a vacuum or low-pressure gaseous environment. Compound materials may be deposited by codeposition.

The five basic techniques are (1) evaporation in a vacuum, (2) sputter deposition, (3) arc-vapor deposition, (4) laser ablation, and (5) ion plating [Brown, 2003]. Evaporation and sputtering are discussed here.

2.4.1.1 Evaporation

Filament-resistive and *electron-beam heating* are the major types of evaporation techniques. Evaporation occurs under ultrahigh vacuum (10^{-9} torr). Filament heating of such metals as copper, gold, chromium, and silver to create a vapor phase is fairly easy and inexpensive. Electron beam heating uses a stream of electrons from a thermionic filament. The electrons are accelerated in an electric field and then directed in a magnetic field to the source material. Electron beams are easily automated, have high evaporation rates and are good for refractory materials. A disadvantage is possible radiation damage to the substrate.

An electron-beam evaporator is shown in Fig. 2.32. The substrate mounting plate is seen in Fig. 2.33. A graphite crucible containing germanium is shown in Fig. 2.34.

2.4.1.2 Sputtering

Sputtering includes *dc* and *RF, magnetron*, and *reactive sputtering* techniques. Sputtering is accomplished when an energetic ion strikes the surface of a sputtering target. Target atoms are dislodged and ejected (recoiled), and become a condensable vapor.

In *dc sputtering*, energetic ions come from plasma usually formed in argon gas. The kinetic energy with which the ion strikes the target determines the *sputter yield*, which is the number of target atoms ejected per incident ion [Mahan, 2000]. A schematic of the dc sputtering process is shown in Fig. 2.35. The target is brought to a negative voltage of 3 to 4 KV. Ionization of the gas occurs and a luminescent cloud forms between the two electrodes. The *positive ions* impinge on the target dislodging atoms. These atoms migrate to the substrate and provide a uniform coating. In addition to lower melting point materials, refractory substances such as Ta, W, Mo, and TiC can be sputtered.

Direct current sputtering is primarily limited to metals and not dielectric materials. Insulating targets cannot quickly drain the positive charge, and as a result, build up a surface charge of positive ions on the front surface of the target. This positive *sheath* repels most of the positive ions, preventing further bombardment and deposition [Brown, 2003].

A sputtering station is shown in Fig. 2.36. The system's vacuum-lock loading chamber is shown in Fig. 2.37.

In *RF sputtering*, a high-frequency voltage is applied across the two electrodes. By alternating the polarization of the target, there is alternate attraction of

Figure 2.32 Electron beam machine (open for setup).

the positive ions that do the sputtering, and the electrons that neutralize the positive surface charge or *sheath.* It is therefore possible to deposit both conductive and dielectric films. The RF sputtering setup is similar to the RIE setup described earlier, and is shown in Fig. 2.38.

Magnetron sputtering is based on the ability to increase the density of an ionized gas by subjecting it to a magnetic field. A *Helmholtz coil* is used to create the magnetic field whose lines are parallel to the target. Electrons wind

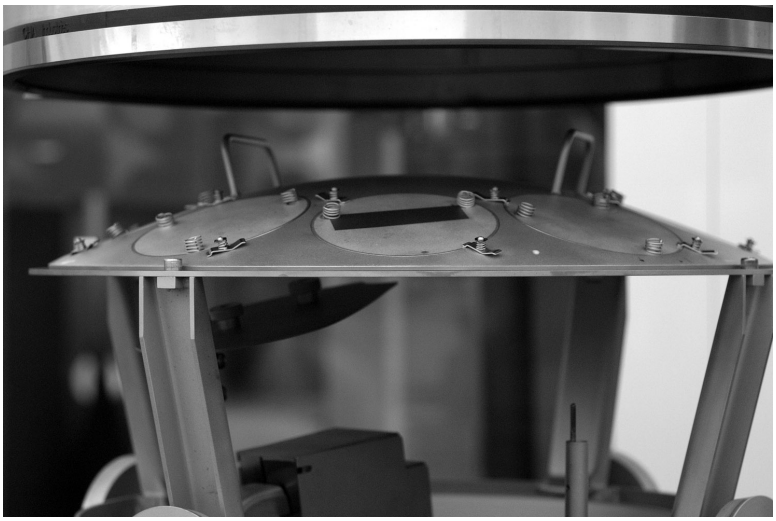

Figure 2.33 Substrate mounting plate.

around the field lines and increase the probability of collisions for ionization near the target. More ions become available for target bombardment resulting in more material being ejected and available for deposition.

In *reactive sputtering* a reactive gas is introduced into the vacuum chamber, where it chemically combines with the depositing film to alter the material's composition and structure. Electrical, mechanical, and optical properties for example may be modified. Stoichiometric oxides, carbides, and nitrides may be deposited.

Figure 2.34 Graphite crucible filled with germanium for evaporation.

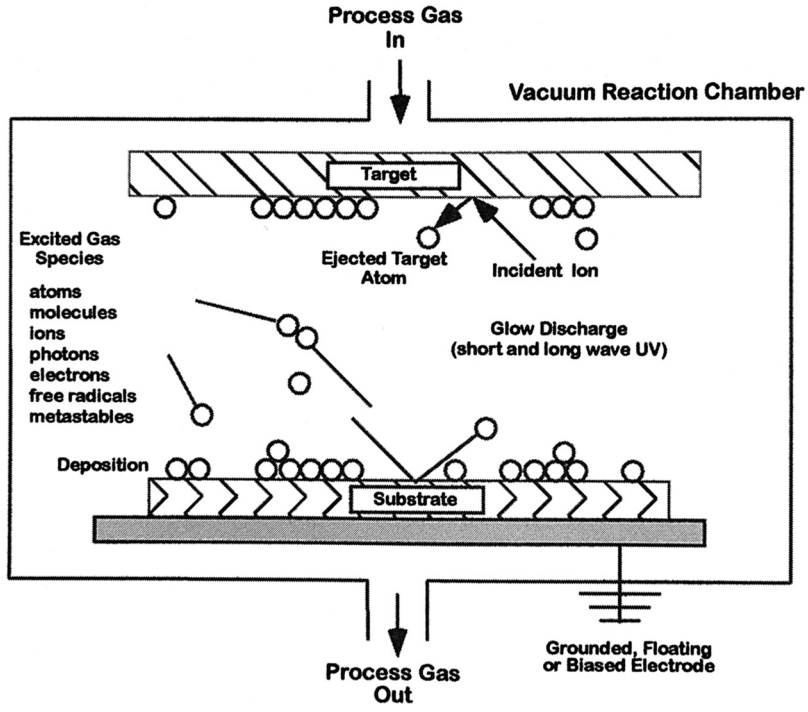

Figure 2.35 Direct current sputtering process. [Reprinted with permission from Brown (2003), copyright Springer.]

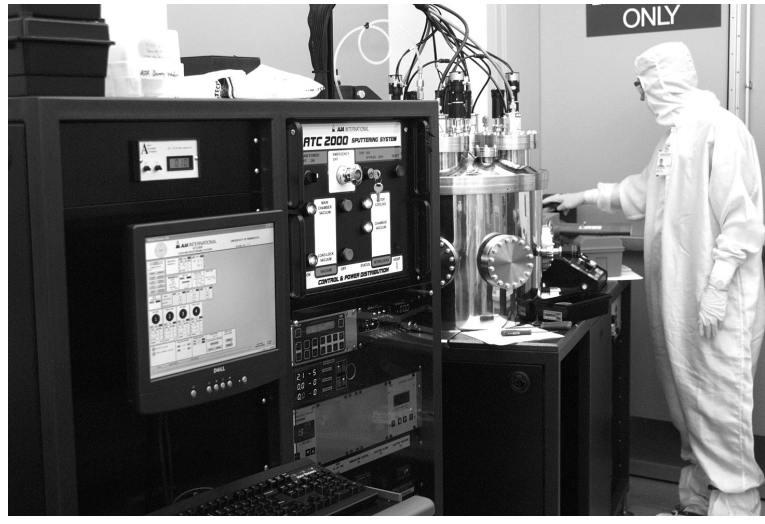

Figure 2.36 Typical sputtering station, with control panel and vacuum chamber.

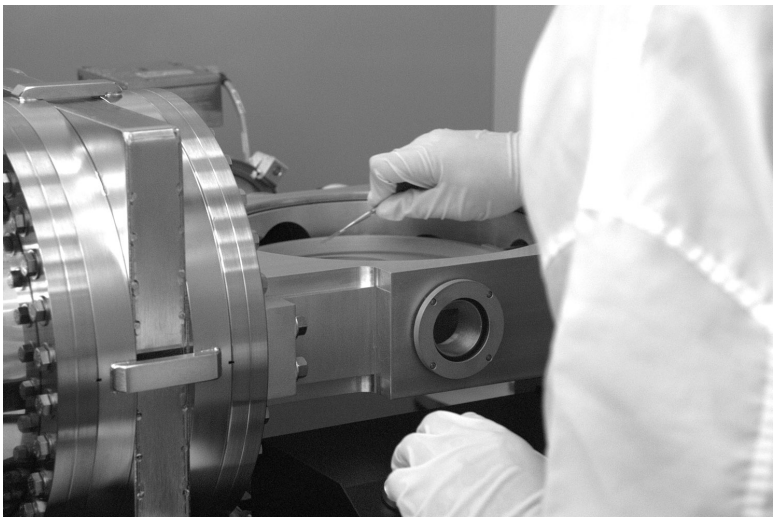

Figure 2.37 Vacuum-lock loading system for the sputtering chamber.

2.4.1.3 Kinetic theory

Thermodynamic and kinetic effects govern the process of PVD, and adsorption and condensation phenomena are important. *Kinetic theory* is used to predict the behavior of gases and vapor. *Condensation* is dependent on the thermal equilibrium vapor pressure of the substances, and determines whether there is a condition of supersaturation at the substrate. *Impingement rate* is the number of collisions z per unit area per second that a gas makes with the substrate or chamber:

$$z = \frac{P}{\sqrt{2\pi mkT}}, \tag{2.8}$$

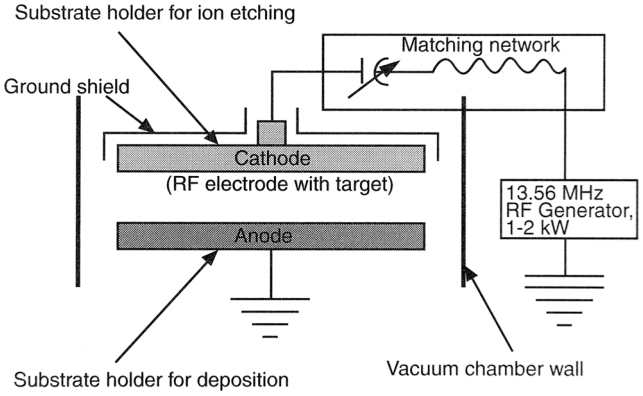

Figure 2.38 Two-electrode diode setup for RF ion sputtering (substrate on cathode target) or sputtering deposition (substrate on anode for deposition. [Reprinted with permission from Madou (2002), copyright Taylor and Francis Group, 2002.]

where

P is the gas pressure,
m is the particle mass,
k is Boltzmann's constant, and
T is the temperature.

2.4.2 Chemical-vapor deposition

Chemical-vapor deposition is the *deposition of a solid* on a heated surface from a *chemical reaction in the vapor phase*, and dates back to the late 1880s for the production of carbon or metal-coated incandescent lamp filaments. Today, applications are primarily in the semiconductor industry. Like PVD, the deposition species are atoms or molecules or a combination of these. Plasma-enhanced chemical-vapor deposition (PECVD) and activated sputtering are combinations of CVD and PVD. A PECVD machine is shown in Fig. 2.39.
Advantages of CVD include:

(1) high throwing power for ease of filling deep recesses, holes, and other 3D shapes;
(2) deposition is not limited to line-of-sight;
(3) coatings of up to several centimeters can be realized;
(4) ultrahigh vacuums are not necessary; and
(5) codeposition of elements or compounds is achievable.

Disadvantages include the use of temperatures above 600°C, requirements for chemical precursors with high vapor pressure and toxicity, as well as toxic by-products.

Figure 2.39 Plasma-enhanced chemical-vapor deposition station.

Thermodynamics and *kinetics* are used to describe the properties of reactants as they reach the deposition surface. The sequence of events are:

(1) reactant gases enter the reactor by forced flow,
(2) gases diffuse through the boundary layer,
(3) gases come in contact with the surface of the substrate,
(4) deposition takes place, and
(5) gaseous by-products are diffused away from the surface (Fig. 2.40) [Pierson, 1999].

There are three factors that control the nature and properties of the deposit: epitaxy, gas-phase precipitation, and thermal expansion. *Epitaxy* is the growth of a crystalline film on a crystalline surface, with the substrate acting as the seed crystal. *Homoepitaxy* implies that the deposit and substrate are identical, and *heteroepitaxy* implies that they are different. Epitaxial growth cannot occur if there are major structural differences. In the latter case, intermediate buffer materials may be used. *Gas-phase precipitation* is the occurrence of CVD in the gas phase rather than on the surface of the substrate, and occurs with supersaturated gases and high temperatures. This is generally not a good thing unless powders are being made. Finally, stress through *thermal expansion* can cause cracking and spalling of the coating as it cools if the coefficient of thermal expansion varies significantly between the deposit and substrate.

Microstructures vary based on the material. Ceramics, including SiO_2, Al_2O_3, Si_3N_4, and most dielectrics are amorphous. Metal deposits tend to be crystalline. CVD structure can be controlled by manipulation of temperature, pressure, supersaturation, and the CVD reaction [Pierson, 1999].

Thermal oxidation of silicon was addressed above. Silicon dioxide films can be fabricated with low-temperature oxidation (LTO), oxidation with

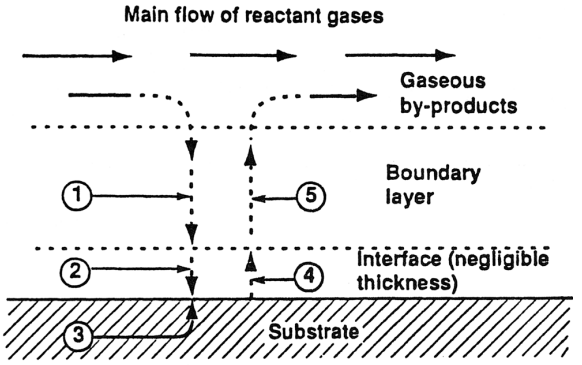

Figure 2.40 Chemical-vapor deposition sequence. [Reprinted with permission from Pierson (1999), copyright William Andrew Publishing.]

tetraethylorthosilicate, $Si(OC_2H_5)_4$ (TEOS), high temperature oxidation (HTO), and with PECVD. Low pressure chemical vapor deposition (LPCVD) of silicon dioxide may occur by reacting silane and oxygen as shown:

$$SiH_4 + O_2 \xrightarrow{500^\circ C} SiO_2 + 2H_2, \tag{2.9}$$

or from dichlorosilane:

$$SiCl_2H_2 + 2H_2O \xrightarrow{900^\circ C} SiO_2 + 2H_2 + 2HCl. \tag{2.10}$$

Silicon nitride can be deposited by LPCVD by reacting dichlorosilane and ammonia:

$$3SiCl_2H_2 + 4NH_3 \xrightarrow{800^\circ C} Si_3N_4 + 6HCL + 6H_2 \tag{2.11}$$

A LPCVD control console is shown in Fig. 2.41, the loading chamber is shown in Fig. 2.42, and an inside look at the mass-flow controllers is shown in Fig. 2.43.

2.5 Ion Implantation

Although used extensively for integrated circuit manufacturing, doping is useful for bioMEMS fabrication in two ways. First, doping of silicon can have beneficial effects for micromachining, and second, integration of electronic and micromachined components become more important with miniaturization of implantable devices. In ion implantation, the dopant element is ionized, accelerated to a kinetic energy of several hundred kiloelecton volts, and then driven into the substrate.

The conductivity of an intrinsic semiconductor can be increased through doping. The *charge carrier density* can be increased through impurities of either higher or lower valence. For example, if pentavalent substitutional atoms P, As, or Sb are placed into a covalently bonded tetravalent material such as Si or Ge, only four of their five valence electrons are required to participate in covalent bonding. The fifth electron remains weakly bound to the impurity or donor atom, and is easily detached. The energy gap between the *donor* and *conducting bands* is much smaller than between the *valence* and *conduction bands*, or the normal *band gap*. The *Fermi level*, which is normally halfway between the conduction and valence bands in an intrinsic semiconductor, becomes higher in the *n*-type extrinsic semiconductor. (When two different substances are brought into contact, such as an *n*-type semiconductor and *p*-type semiconductor, electrons flow until the Fermi levels of the two substances are at the same energy.)

The addition of a trivalent element such as B, Al, Ga, In, and Tl to Si or Ge creates a *p*-type extrinsic semiconductor. Here the deficit in bonding electrons creates a *hole* (or moving positive charge) that accepts an electron from elsewhere in the crystal. Thus, the Fermi level becomes lowered in the *p*-type extrinsic semiconductor [Mitchell, 2004].

Anisotropic etchants such as potassium hydroxide (KOH), ethylene diamine pyrochatechol (EDP), and tetramethyl ammonium hydroxide (TMAH) attack silicon preferentially along preferred crystallographic directions (described below), and show a reduction of etch rate in heavily doped *p*-type regions. For this purpose boron is typically incorporated using ion implantation.

Figure 2.41 Low-pressure chemical-vapor deposition system (LPCVD).

2.6 Wet-Bulk Surface Micromachining

In wet-bulk micromachining, features are sculptured in bulk materials like silicon, quartz, sapphire, ceramics, SiC, GaAs, InP, and Ge by orientation-independent (isotropic) or orientation-dependent (anisotropic) wet etchants.

Figure 2.42 Loading chamber for the LPCVD system.

2.6.1 Silicon wafers

Integrated circuits typically have aspect ratios of 1:2, while in bioMEMS the ratio may be up to 400. Crystalline-silicon substrates are available as circular wafers of varied diameters, including 100 mm (4 in.) and 150 mm (6 in.), which are more

Figure 2.43 Mass-flow controllers for the LPCVD system.

practical for MEMS and bioMEMS devices. Larger sizes are commonly used in integrated circuit manufacturing. Standard thicknesses for the 100-mm wafer are 525 μm, and for the 150-mm wafer 650 μm. Double polished wafers are 100 μm thinner.

In the *Miller indices* that were introduced earlier, planes are described with parenthesis, e.g., (100), (110), and (111). A particular direction is described with square brackets, e.g., [100], and is normal to the plane; e.g., the [100] direction is

perpendicular to the (100) plane. Because of the symmetry, there are many [100] directions. The set of equivalent directions is designated with angle brackets: ⟨100⟩. The set of equivalent planes is described with braces: {100}.

Figure 2.44 shows an illustration of primary and secondary flats of {100} and {111} wafers for both *n*-type and *p*-type doping, and various planes in wafers of {100} orientation are identified [Maluf, 2000].

2.6.2 Isotropic and anisotropic etching

Wet-bulk micromachining of wafers can be used for cleaning, shaping 3D structures, removing surface damage, polishing, and characterizing. Parameters include undercutting (bias), tolerance, etch rate, anisotropy, selectivity, overetch, feature-size control, and loading effects. Temperature control and stirring are important. Isotropic etchants are applied in all crystallographic directions at

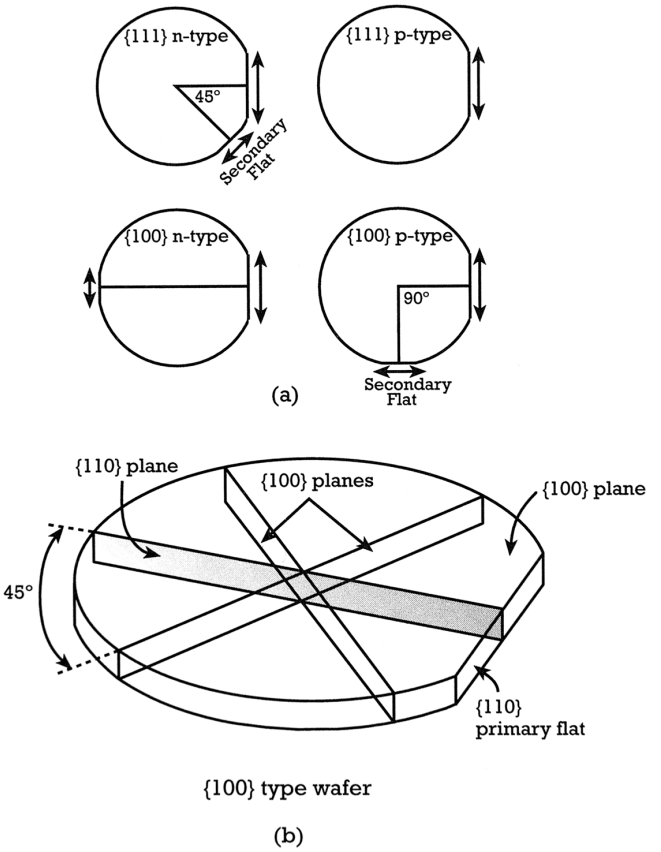

Figure 2.44 (a) Primary and secondary flats of {100} and {111} wafers for both *n*-type and *p*-type doping; (b) various planes in a {100}-orientation wafer. [Reprinted with permission from Maluf (2000), copyright Artech House.]

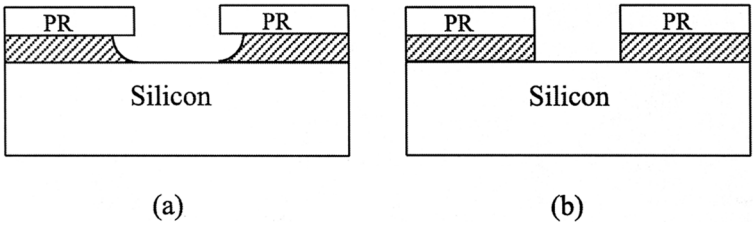

Figure 2.45 Diagram showing the differences in (a) isotropic versus (b) anisotropic etching. [Reprinted with permission from Baldi and Ziaie (2004), copyright Elsevier.]

the same rate, are usually acidic, and lead to rounded features. Alkaline chemicals etch anisotropically, etching at different rates depending on the exposed crystal orientation.

Figure 2.45 shows the difference between isotropic and anisotropic etching. Isotropic agents are diffusion limited, while anisotropic agents tend to be rate-limited. Both involve oxidation of the Si followed by dissolution of the hydrated silicate. Isotropic etching is used for removal of work-damaged surfaces, rounding sharp corners to avoid stress concentration, removing roughness, thinning, patterning single crystal, polycrystalline or amorphous films, and delineation of electrical junctions. Isotropic etching with HNA [HNA = HF (hydrofluoric acid) + HNO_3 (nitric acid) + CH_3COOH (acetic acid)] proceeds as shown:

$$\mathrm{Si} + \mathrm{HNO_3} + 6\mathrm{HF} \longrightarrow \mathrm{H_2SiF_6} + \mathrm{HNO_2} + \mathrm{H_2O} + \mathrm{H_2} \qquad (2.12)$$

(H_2SiF_6 is water soluble).

Anisotropic wet etching takes place in the presence of hydroxide groups:

$$\mathrm{Si} + 2\mathrm{OH^-} \longrightarrow \mathrm{Si(OH)_2^{2+}} + 4\mathrm{e^-}, \qquad (2.13)$$

$$4\mathrm{H_2O} + 4\mathrm{e^-} \longrightarrow 4\mathrm{OH^-} + 2\mathrm{H_2}, \qquad (2.14)$$

$$\mathrm{Si(OH)_2^{2+}} + 4\mathrm{OH^-} \longrightarrow \mathrm{SiO_2(OH)_2^{2-}} + 2\mathrm{H_2O}, \qquad (2.15)$$

and

$$\therefore\ \mathrm{Si} + 2\mathrm{OH^-} + 2\mathrm{H_2O} \longrightarrow \mathrm{Si(OH)_2^{2+}} + 2\mathrm{H_2}. \qquad (2.16)$$

Anisotropic etching results in geometric shapes bounded by the slowest etching plane. Etching profiles for {100}-orientation silicon is shown in Fig. 2.46; and {110}-orientation silicon wafer in Fig. 2.47. Figure 2.48 shows anisotropic wet etching of convex corners and a suspended beam.

2.6.3 Selection of silicon wafer orientation

Selection of wafer type depends on the design requirements. The [100]-orientation silicon has inward sloping walls of 54.74 deg that tend to use up room; flat

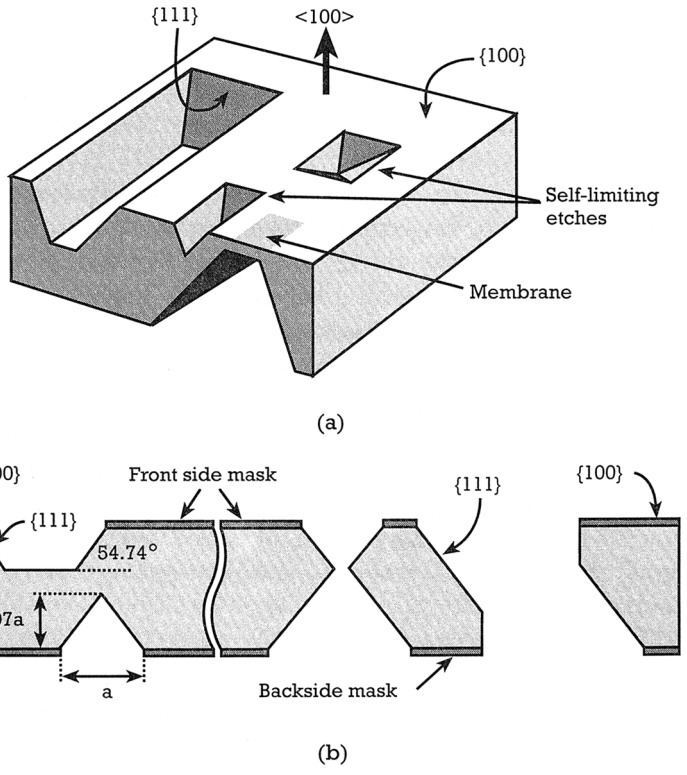

Figure 2.46 Anisotropic etching of cavities in {100}-oriented silicon: (a) cavities, self-limiting pyramidal and V-shaped pits, and thin membranes, and (b) etching from both sides creating vias. [Reprinted with permission from Maluf (2000), copyright Artech House.]

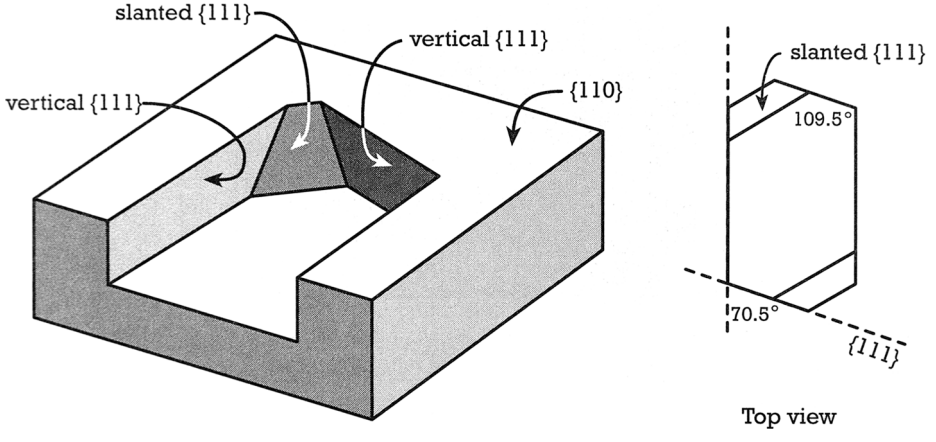

Figure 2.47 Anisotropic etching in {110}-oriented silicon. Etched structures are delineated by four vertical {111} planes and two slanted {111} planes. [Reprinted from Ammar (1980), copyright IEEE.]

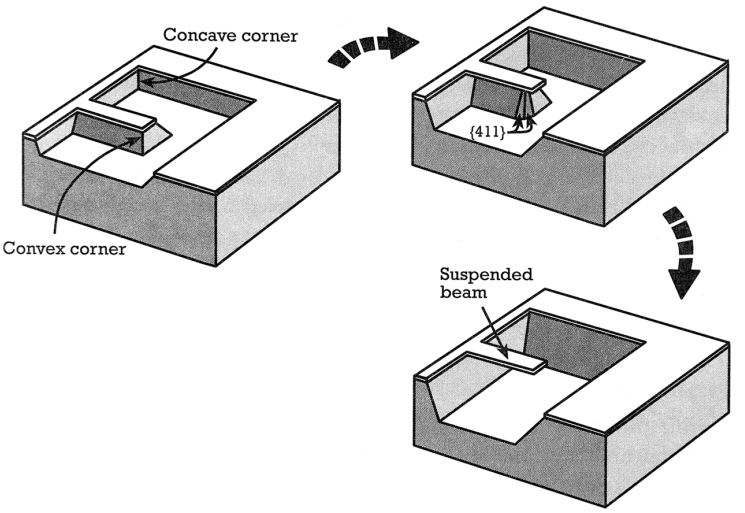

Figure 2.48 Etching a convex corners and formation of a suspended beam. [Reprinted with permission from Maluf (2000), copyright Artech House.]

bottoms that are parallel to the surface and ideal for membrane fabrication; bridges that are perpendicular to a V-groove bound by (111) planes that cannot be undercetched; shape and orientation of diaphragms that are convenient and simple to design; and diaphragm sizes, bounded by nonetching {111} planes, are easier to control.

In contrast, the [110]-orientation silicon has vertical {111} walls; narrow trenches with a high aspect ratio; multifaceted cavity bottoms that make for poor diaphragms ({110} and {100} planes); bridges that are perpendicular to a V-groove bounded by (111) planes that can be undercut; diaphragm's shape and orientation that are awkward and more difficult to design; and diaphragm size that is difficult to control.

2.6.4 3D structures with sacrificial layers

The techniques discussed above are all forms of surface micromachining. They are the primary tools of the micromachinist, rather than lathes, drills, mills, saws, and the usual hand tools of a general machinist. But like the machinist, the micromachinist must produce 3D components, and in terms of hard fabrication techniques, this requires use of sacrificial layers, or layers that can be etched away to leave undercut features. These include cantilever parts, free-moving masses, bridges, and diaphragms.

In 3D surface micromachining, features are built up layer by layer. Dry etching defines the surface feature in the *x*-*y* plane, and wet etching releases them from the plane by undercutting. Shapes are unrestricted by the crystallography of the

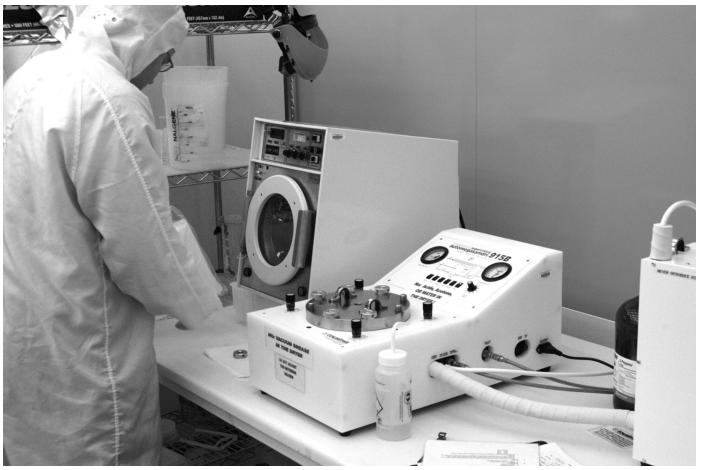

Figure 2.49 Critical point drier.

substrate. Polysilicon is the main structural element, deposited as amorphous silicon and annealed at about 580°C. A disadvantage is that LPCVD polysilicon films are thin, and there are dimensional uncertainties without the crystallographic control. Wet release processes cause stiction, or sticking of suspended structures to the substrate. Stiction can be minimized by use of a critical point drier as shown in Fig. 2.49. The critical point occurs at a specific temperature, pressure, and density such that there is no apparent difference between the liquid and gas state.

The process requires for example phosphosilicate glass (PSG) or polysilicon films being deposited on a silicon dioxide layer, with the latter serving as a sacrificial layer. The process steps for creating free-standing polysilicon bridge are structured as seen in Fig. 2.50.

Another process is *silicon on insulator* (SOI). Here a single crystal epilayer is used and surface features of up to 100 μm are obtainable. Its advantages include more reliable and reproducible sensors, and frequently less process steps. Hexagonal honeycomb polysilicon (HEXSIL) is yet another process that enables fabrication of tall 3D structures [Madou, 2002; Varadan et al., 2001].

2.6.4.1 Structural elements

Common structural elements include polysilicon, polyimide, silicon nitride, and tungsten. The polysilicon and its sacrificial layer, silicon dioxide, are applied by LPCVD. Silicon dioxide is etched away with HF solution without etching the polysilicon. Polyimide can be used with aluminum as the sacrificial layer, which is dissolvable with acid-based etchants.

Silicon nitride is both a good structural material and electrical insulator. Polysilicon can be used as the sacrificial layer, in which case KOH and EDP can be

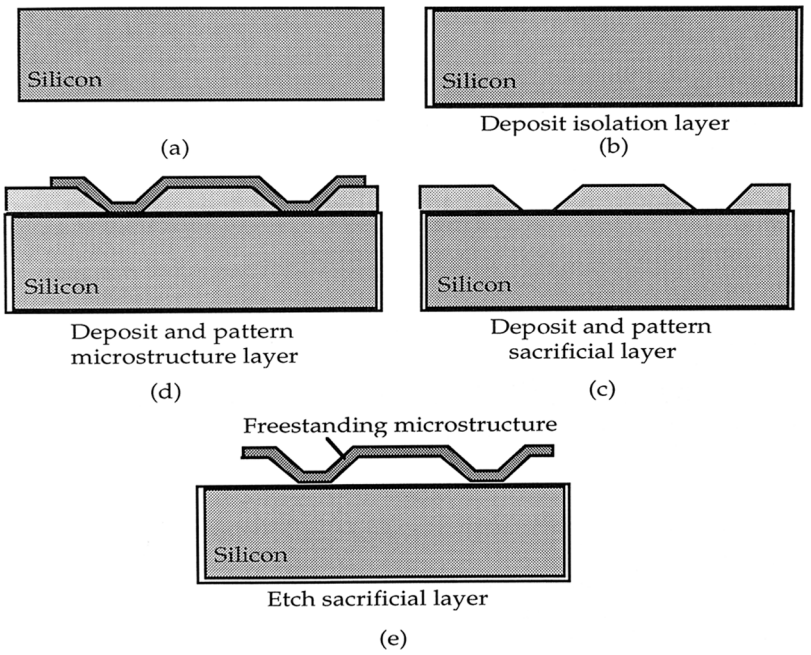

Figure 2.50 Creating a freestanding structure by use of a sacrificial layer. [Reprinted with permission from Tabib-Azar (1998), copyright Springer.]

used as the etchants. Tungsten can be applied by CVD over silicon dioxide, and again HF is a suitable etchant to remove the silicon dioxide sacrificial layer [Varadan et al., 2001].

2.6.4.2 Stress and strain

Properties of a thin film may be different than its bulk properties with smaller grains and higher surface-to-volume ratio. Structural mechanics deals with *elasticity* of materials. *Stress* is defined microscopically as the *force per unit area* acting on the surface of a differential volume element of a solid body. Stresses acting perpendicular to the surface are called *normal*, and those acting along the sides of a surface are *shear. Strain* is the differential *deformation* of a solid body in response to a force (change in length per original unit length, hence strain is dimensionless).

To understand the free-standing structures produced by surface micromachining, it is necessary to consult mechanical property data for the selected materials, and to calculate thermal, intrinsic, and extrinsic stress that may be present. Moreover, understanding the behavior of cantilevers, beams, and other structures requires modeling the bending-type deformations, reaction forces, and moments. These are issues are discussed thoroughly by Senturia (2001).

2.7 Dry-Bulk Surface Micromachining

2.7.1 Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) is a method for building high-aspect-ratio micromachined parts, and may be used to make high-aspect micromolds. Plasma sources include *inductively coupled plasma* and *electron-cyclotron resonance*. Etch rate is diffusion limited and decreases with increasing aspect ratio.

Inductively coupled plasma is generated by a helical resonator combined with an electrostatic shield to produce electric field lines that are circumferential in response to the axial RF magnetic field. The power source is driven at 13.56 MHz, producing a high-density, low-pressure, and low-energy plasma.

Electron-cyclotron resonance uses a microwave source, waveguide, magnetic field, and quartz chamber filled with gas at low pressure. The interaction of the microwave and magnetic fields produces intense high-density plasma to which the silicon wafer is exposed.

High-aspect-ratio etching is achieved by the Bosch process. Glow discharge processes have a tendency to create polymeric species by chemical cross-linking. The deposition of this material is typically slower than its removal, and the etching is stopped, or *passivated*, by this layer. The Bosch process takes advantage of this by *alternating* etching and passivation allowing deeply etched trenches (Fig. 2.51). Microscopically, this can be seen as a scalloped

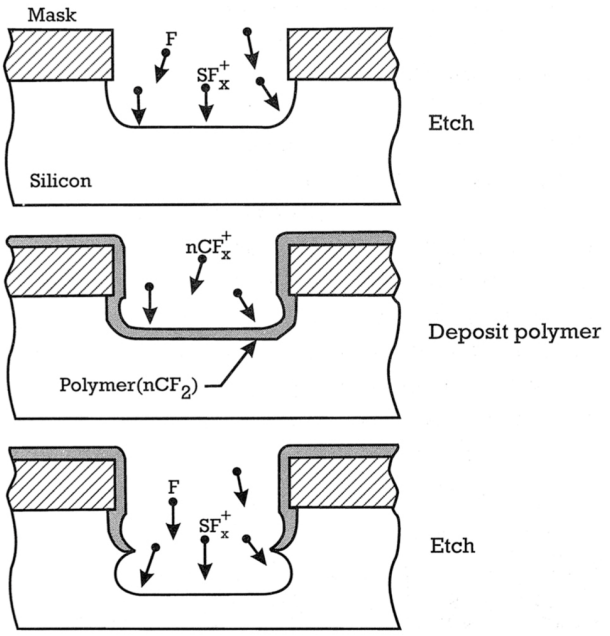

Figure 2.51 Deep reactive ion etch (DRIE) profile using the Bosch process. The process cycles between SF_6 gas etching and C_4F_8 polymer deposition. [Reprinted with permission from Maluf (2000), copyright Artech House.]

Figure 2.52 Deep reactive ion etching (DRIE) machine.

appearance of the side wall. SF_6 plasma is used for etching, while C_4F_8 is used for passivation.

In bioMEMS for example, this technique could be useful for creating channels in silicon for microfluidic use. After the deep trenches are formed, a clear glass plate could be anodically bonded to the silicon substrate converting trenches into channels. A DRIE machine is shown in Fig. 2.52.

DRIE techniques have been used in a diversity of applications, including the production of nanowires for molding to make nanocapillaries [Doherty et al., 2003], the manufacture of micromirrors used for laser beam scanning in an endoscopic optical coherence tomography (OCT) system [Xie et al., 2003], and etching chambers for a silicon-based peristaltically actuated implantable medical drug delivery system consisting of three pumping chambers [Ridgeway et al., 2002].

DRIE techniques were also required to fabricate high-aspect-ratio nozzles for a nanoelectrospray device for delivery of the sample to the mass spectrometer [Corso et al., 2001], to etch silicon and aluminum membranes for piezoelectric aluminum-nitride thin-film ultrasonic transducers [Valbin and Sevely, 2001], and to produce new a type of piezoelectric micro-array jet for drug delivery [Yuan et al., 2003].

2.7.2 Single-crystal reactive etching and metallization (SCREAM)

Single-crystal reactive etching and metallization (SCREAM) is a low temperature process that may be useful for hybrid integrated-circuit devices and bioMEMS. The SCREAM process yields high-aspect-ratio (50:1) released, single-crystal silicon structures with micrometer-scale minimum features and a suspension span

of greater than 5 mm [MacDonald, 1996; Shaw et al., 1993; Tay et al., 2000]. A recent summary and illustration of the process was published by Ziaie et al. (2004).

2.7.3 LIGA and UV-LIGA

LIGA is a German acronym that translates into English as lithography electroplating molding. This high-aspect-ratio process requires high-energy synchrotron radiation lithography of a thick resist layer. The exposed areas are electroplated with metal, and the resist is then removed. Figure 2.53 shows the LIGA process. The vertical walls produced can be a few microns to a few millimeters high. The electroplated substrate then serves as a either a part or mold for soft fabrication techniques [Kupka et al., 2000; MacGeough et al., 2001; McCormick et al., 1994]. Because access to synchrotron radiation is difficult, DRIE may be preferred, or an analogous process called UV-LIGA may be used. In the latter, special thick resists that allow deep ultraviolet penetration and reaction are used [Wenmin et al., 1998]. A LIGA-like process using an intense beam of light from an excimer laser has been used to pattern material directly, and has been used to create a micro-carrier for molecular transport [Chang et al., 2004].

LIGA has been used for a number of bioMEMS devices, including fabrication of continuous flow polymerase chain reaction (CFPCR) microfluidic devices in polycarbonate [Hupert et al., 2003; Mitchell et al., 2003], and radial microturbines, which can be integrated onto minimally invasive surgical tools [Wallrabe et al., 1996].

2.8 HEXIL Process

The HEXIL process is shown in Fig. 2.54, where the process begins with DRIE processing of the silicon substrate. The scalloped sidewalls are then wet-etched isotropically to create smooth surfaces, thus creating a silicon mold that may be used repeatedly in the steps that follow. PSG is then applied as a sacrificial layer, and the trenches are then filled by chemical-vapor deposition of (CVD) of polysilicon creating the first structural layer, as demonstrated. The substrate is then annealed and polished, and another structural layer is patterned and deposited such that it physically connects the structures of the first layer. The entire structure is then released in buffered hydrofluoric acid.

In Chapter 5 it is shown how the HEXIL process may be used to fabricate channels.

2.9 Electroplating

Electroplating provides thicker layers of metal structures than the previously described thin-film techniques.

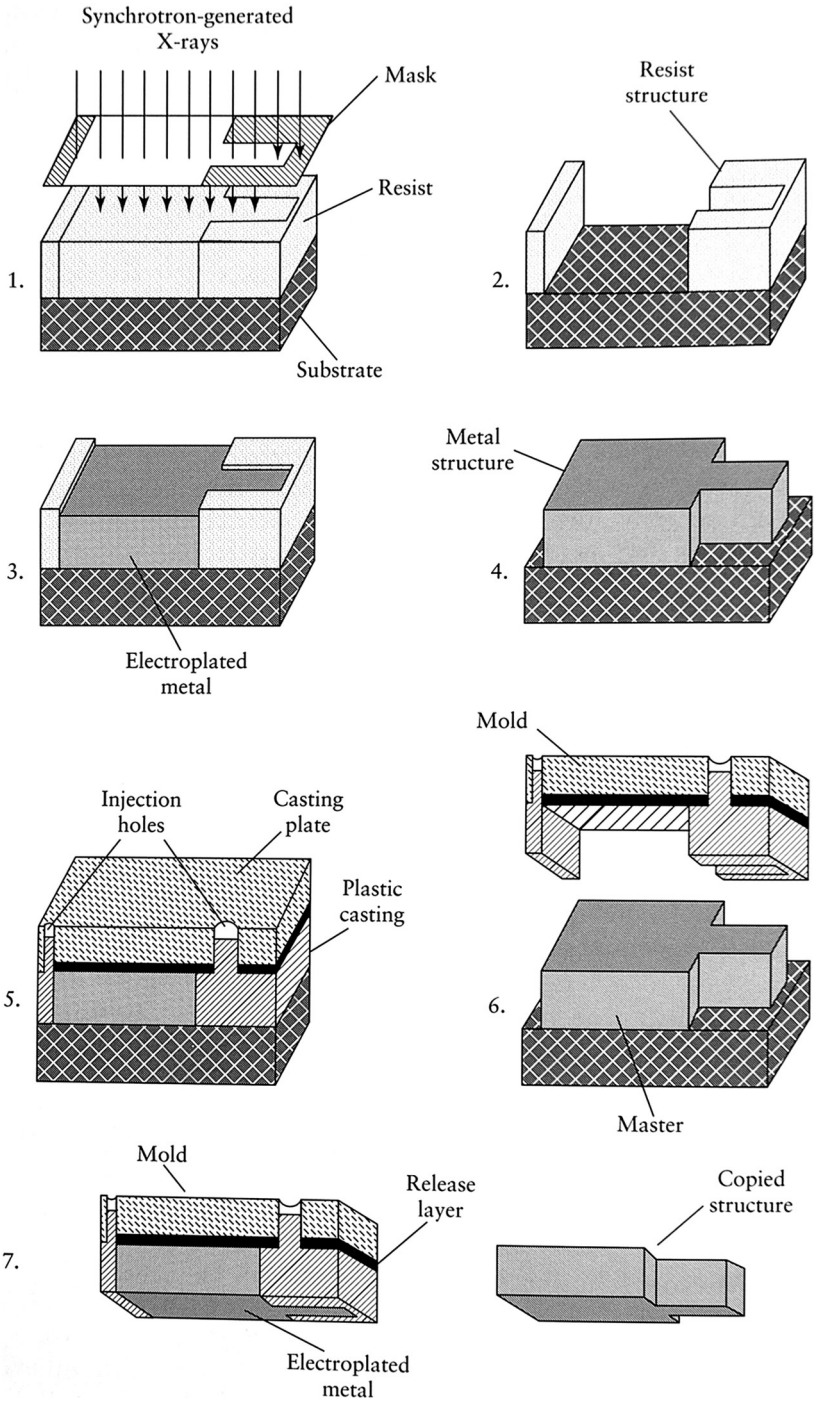

Figure 2.53 LIGA process. [Reprinted with permission from Fatikow and Rembold (1997), copyright Springer.]

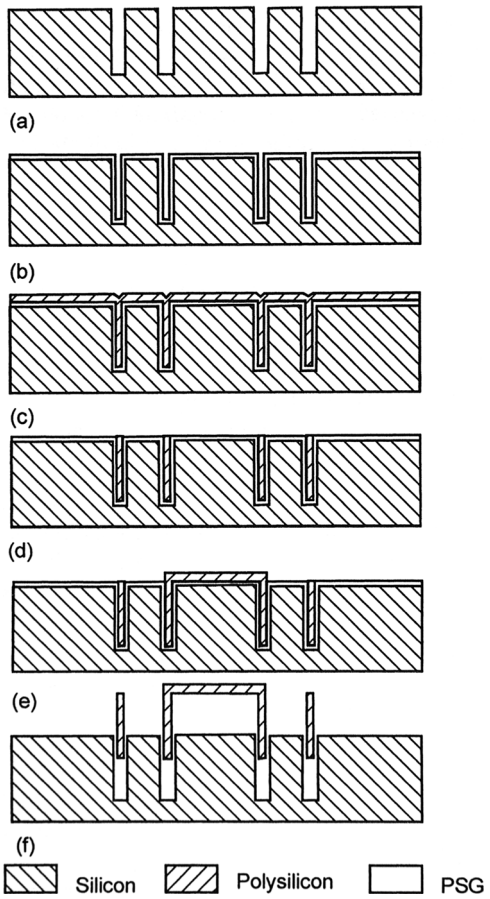

Figure 2.54 HEXIL process steps. (a) DRIE processing of the silicon substrate, (b) PSG is applied as a sacrificial layer, (c) the trenches are then filled by chemical-vapor deposition of (CVD) of polysilicon creating the first structural layer, (d) the substrate is then annealed and polished, and (e) another structural layer is patterned and deposited such that it physically connects the structures of the first layer. [Reprinted with permission from Nguyen and Wereley (2002), copyright Artech House.]

The substrate is placed into a solution of the desired metal ions and serves as the negative cathode. The positive anode is typically made of the desired metal to be deposited (commonly nickel). When current is applied, ions are reduced at the substrate surface, become insoluble, and are deposited onto the substrate surface.

Electroplating techniques for bioMEMS devices are well represented in the literature. Nickel electroplating can be used to fabricate 3D parts from photoresist molds [Pai et al., 2002] and to make hot embossing molds for polymer fabrication [Aristone et al., 2003]. Nickel-cobalt electroplated microneedle arrays have been fabricated on silicon wafers [Liu et al., 2001]. These metallic microneedles

with annular structures may be combined with a micropump for drug delivery and *in-situ* physiological fluid sampling. The mechanical strength inherent in the alloy provides excellent durability for the needles. Arrays of one to ten pipettes have been fabricated using electroplated nickel as the structural material, and palladium used as the biocompatible coating of inside walls [Papautsky et al., 2000].

Electroplated permanent magnetic arrays have been developed for a novel bidirectional magnetic microactuator [Cho and Ahn, 2002]. Catheters that have bending, torsional, and extending functions for medical applications consisting of a shape-memory alloy (SMA) coil and a stainless-steel-liner coil have been developed. The SMA coil and the liner coil are connected using nickel electroplating and acrylic resin electrodeposition, which allows for low-cost assembly [Haga et al., 2000].

A new integration concept based on an additive electroplating technology (AET) is described by Binder and Benecke (1999). With this technology, the integration of fixed and movable electroplated microstructures are placed on top of a standard ASIC by a low-temperature back-end process.

Increasing rigidity of structures for coils and vascular stent use is described with electroplating by Rogers et al. (1997). The method begins with generating thin patterns of metal produced by micro-contact printing on curved substrates. Electrodeposition is then used, increasing the thickness and rigidity of these structures. Removal of substrate results in freestanding 3D objects.

2.10 Substrate Bonding

Many applications require bonding of substrate materials. For example, bonding silicon to glass allows for the creation of enclosed channels with viewports for the addition of detectors; thus, complex 3D structures can be fabricated. Several techniques are employed, including *silicon-direct bonding* for silicon-to-silicon fusion (and SOI), *anodic bonding* for silicon-to-glass bonding, and use of intermediate adhesive layers.

To bond silicon to silicon, the cleaned surfaces are chemically rendered hydrophilic, and brought tightly together, attracted by van der Waals forces and subsequent high-temperature annealing. Silicon is bonded to glass (Pyrex 7740 has matching thermal expansion to silicon) by compression and heating to 300–400°C, then applying about 1000 V of direct current across the composite, with the glass as the negative cathode and the silicon as the positive anode (Fig. 2.55).

Adhesive residues, low bonding strength, heating of entire parts during joining, and poor long-term stability are disadvantages of these conventional techniques. Lasers are emerging as useful tools for joining miniaturized devices. The beam can be focused to less than .001 double prime, allowing localized joining of very small geometries. There is minimal heat input into the part so distortion and change in material properties is minimal. The high quality of the laser welds and the precise process control enable hermetic sealing [Witte et al., 2002].

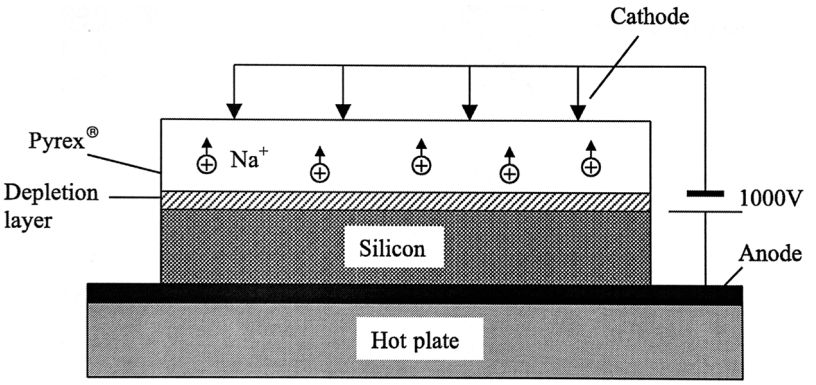

Figure 2.55 Anodic bonding. [Reprinted with permission from Baldi and Ziaie (2004), copyright Elsevier.]

Additional bonding applications include packaging [Najafi, 2003], sealing pump chambers [Ridgeway et al., 2002], and adjoining Venturi pumps to REI-etched silicon channels for bidirectional microfluidic regulation [Chang et al., 2002].

2.11 Review Questions

1. Describe what is meant by hard versus soft fabrication in terms of the materials.
2. What photolithography steps are necessary to prepare a silicon wafer for etching or chemical vapor deposition?
3. Describe various methods for producing silicon-dioxide films on silicon wafers.
4. What is the difference between a positive and negative resist? Give examples of each.
5. What ultraviolet light wavelength in nanometers is the g-line?
6. What is the equation for the theoretical limits to resolution? Define your variables.
7. List and describe the various methods for etching silicon.
8. Describe physical vapor deposition and chemical vapor deposition.
9. How is doping of silicon useful when etching?
10. Describe the chemical processes behind isotropic and anisotropic etching.
11. What design considerations exist when selecting a specific silicon wafer orientation?
12. What is meant by sacrificial layer? Give an example using process steps for creating a cantilever?
13. What structural materials are used for surface micromachining? Identify the associated sacrificial layer materials and etchants.
14. Define stress and strain.

15. Describe deep reactive ion etching (DRIE), including energy sources and uses.
16. What are LIGA, UV-LIGA, and LIGA-like processes?
17. Describe how electroplating works, and give some examples of applications.
18. How is substrate bonding accomplished, and what are the limitations?

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